WUXGA-R5

1920 X 1200 LOW-POWER COLOR XL AMOLED MICRODISPLAY

DATASHEET
Revision A

For Part Numbers:
EMA-100810-01 (color microdisplay)

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Revision Level	ECN	Date	Scope
-	000201	02-2017	Initial Release
A	001083	01-2021	Added timing information for 2 pixels per clock source video timing in 6.1.1

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1. INTRODUCTION

The WUXGA-R5 Color OLED-XL device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high resolution, high image quality, compact size, and very low power. Combining a total of 7,138,368 active dots, the WUXGA-R5 display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

The WUXGA-R5 is backwards compatible with the EMA-100820-01, which is the first version of eMagin Corporation's WUXGA-R5 color microdisplay. The R5 version has been re-designed to enhance manufacturability as well as a few performance characteristics related to power-on sequence and operation at higher luminance levels. Details of the differences between the two versions are documented in eMagin Corporation document 1000147, available upon request.

The active array is comprised of 1944 x 1224 square pixels with a 9.6-micron pitch and a 71% fill factor. An extra 24 columns and 24 rows (beyond the 1920 x 1200 main array) are provided to enable the active WUXGA-R5 display to be shifted by steps of 1 pixel in the X and Y directions for optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 3.2 x 9.6 micron identical sub-pixels, which together form the 9.6-micron square RGB color group. Three primary color filter stripes are applied in alignment with the sub-pixels on a white-emissive OLED layer to form the color display.

The WUXGA-R5 design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. In addition to its flexible matrix addressing circuitry, the WUXGA-R5 includes an internal 10-bit DAC that ensures full 256 gamma-corrected gray levels, an on-chip set of look-up-tables for digital gamma correction, and a novel pulse-width-modulation (PWM) function that, together with the standard analog control, provides an extended dimming range. The PWM function also enables an impulse drive mode of operation that significantly reduces motion artifacts in high speed scene changes.

The WUXGA-R5 includes a very low-power, low-voltage-differential-signaling (LVDS) serialized interface for video data transport that minimizes the number of board interconnections and connector size, reduces electromagnetic emissions (EMI), and enables a lightweight and flexible cable link to a remote video source. Compatibility with standard LVDS drivers simplifies the system integrator's task.

Detailed device specifications and application information for the WUXGA-R5 OLED-XL microdisplay produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION

2.1 WUXGA-R5 Color XL Microdisplay

Display Type:	Emissive, Color AMOLED on Silicon
Format:	1920(x3) x 1200 pixels
Total Pixel Array:	1944(3) x 1224 pixels
Color Pixel Aspect Ratio:	9.6-micron Square
Color Pixel Arrangement	R, G, B, Vertical Stripe
Fill Factor	71%
Viewing Area	18.7 x 11.75 mm (22.1 mm diagonal (0.856"))
Mechanical Envelope	26.4 x 17.5 x 4.72 mm (w x l x h)
Weight	<3 gm
Gray Levels	256 levels per primary color
Uniformity	> 85% end-to-end uniformity
Pixel Spatial Noise	<5% (1 STD)
Contrast Ratio	>1,000:1
Pixel Response	Linear with input video signal (using internal gamma LUT)
Dimming Ratio	>200:1 analog, >500:1 pwm, >50,000:1 total
White Luminance (color display)	>150 cd/m^2
CIE White point	cie-x = 0.27 to 0.37, cie-y = 0.32 to 0.38
Video Modes	WUXGA, HD1080, UXGA, 8-bit control of active window Progressive & Interlaced scan Horizontal (left/right) and vertical (up/down) scan control Frame/field sequential stereovision support Horizontal and vertical image shift by up to 24 pixels Variable row duty rate control
Video Interface	Serialized LVDS, 24b Digital RGB (8 twisted line pairs)
Refresh Rate	30 to 85Hz
Video Source Clock	220 MHz max
LVDS Clock	442 MHz max
LVDS Data Rate	883 Mbps
Control Interface	3.3V to 5V I^2C serial interface
Power Consumption	<350 mW typical @ 150cd/m^2 (1W max)
Power Supply	
VAN (analog & array)	5VDC ±5% (150 mA maximum)
VDD (logic & I/Os)	1.8VDC ±5% (30 mA maximum)
VPG	-1.5VDC ±5% (1 mA maximum)
Operating ambient temperature	-45 to +70°C
Storage temperature	-55to +90°C
Humidity	85%RH non condensing

3. FUNCTIONAL OVERVIEW

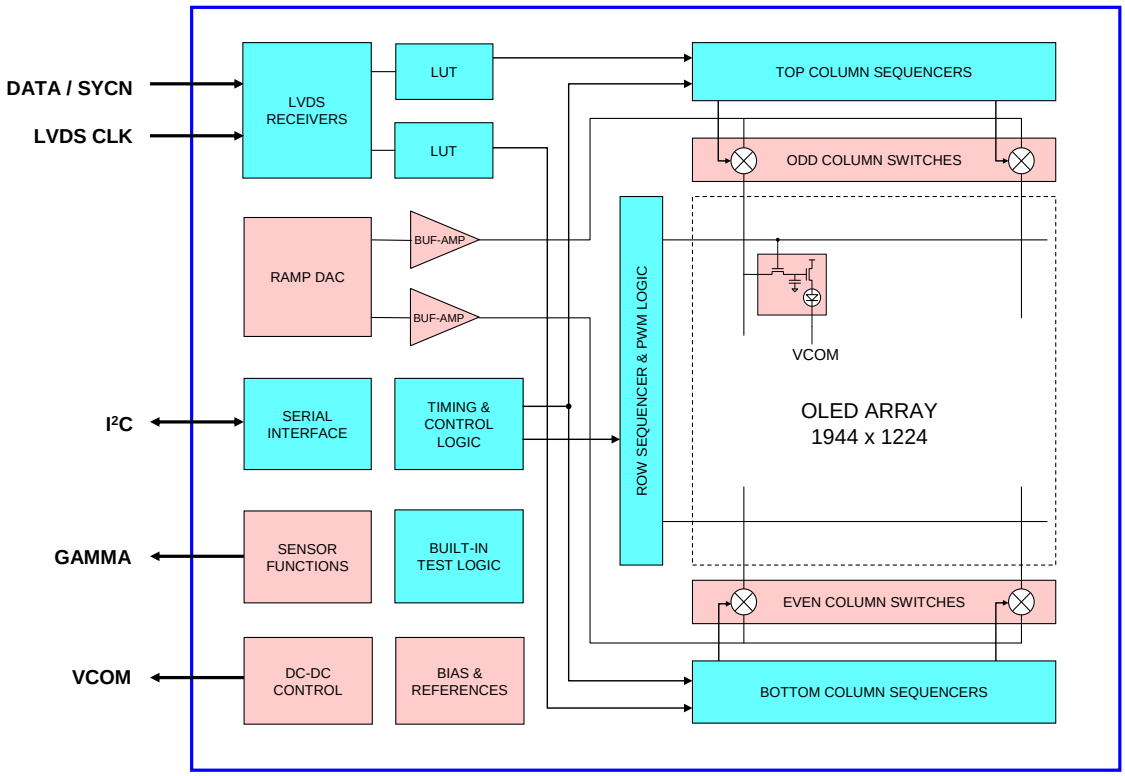


Figure 1 : Top-level block diagram for WUXGA

The top-level block diagram for the WUXGA-R5 microdisplay is shown in Figure 1. Bi-directional row and column sequencer circuits are used for addressing individual cells within the 1944 x 1224 pixel array, and internal digital-to-analog conversion circuits are included for converting the digital input data into the analog signals needed for programming the pixels. A storage element (capacitor) resides at each pixel cell that is used to set the gray level.

Odd columns are driven by data sequencers located at the top of the array and even columns by bottom side sequencers. To obtain a linear gray-scale response from the OLED pixels the digital input data must be formatted with Gamma correction. This is achieved with an on-board gamma LUT which is programmed via the serial interface with data generated externally.

2 x 24-bit RGB data (two pixels per clock), synchronization signals, and the system clock are fed to the microdisplay via a low-power LVDS interface comprised of 8 twisted line pairs. This is illustrated in the interface block diagram given in Figure 2.

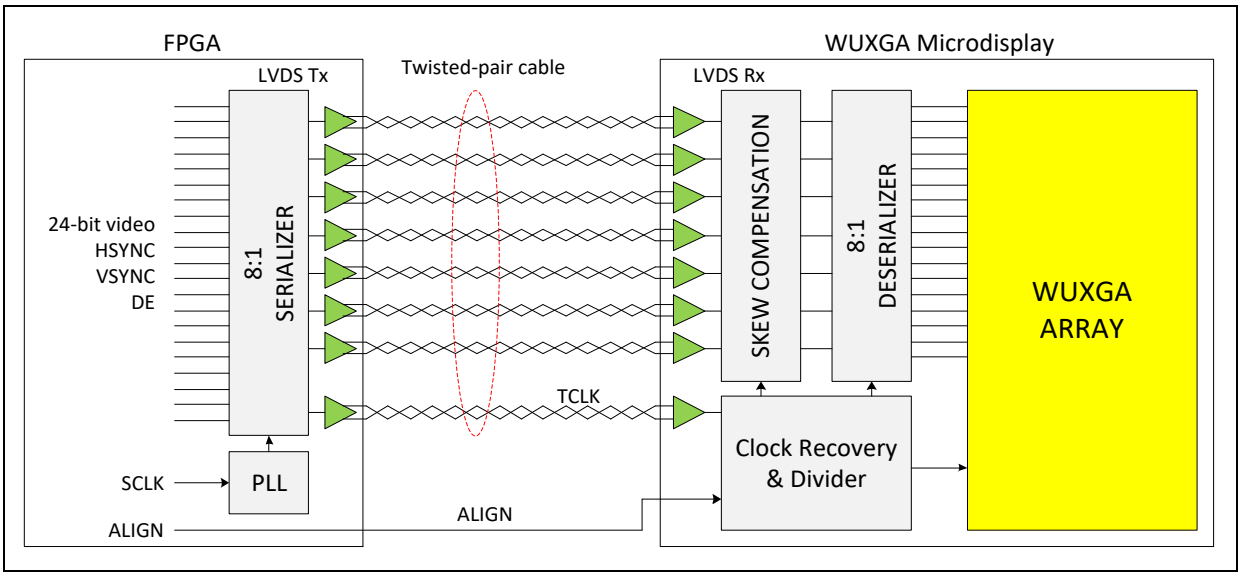


Figure 2: LVDS interface diagram

The externally generated pixel clock and sync signals for various video formats are converted into individual control signals by the internal timing logic block. Several standard video formats are supported by the sequencer circuits to simplify external driving requirements. These include:

- WUXGA-R5 – non-interlaced and interlaced
- HD1080 – non-interlaced and interlaced
- UXGA – non-interlaced and interlaced
- Stereovision – frame and field sequential mode following VESA standard
- Frame rates – 30 to 85Hz, using externally provided timing

Each OLED diode in the array matrix is actively driven to the desired luminance level with 8-bit accuracy by its individual pixel drive circuit. The pixel is refreshed once every frame period (or every second period in stereo mode) and then the analog signal is held on a storage capacitor between refresh cycles.

A number of sensor signals are provided by the backplane for setting and regulating the display performance. These include a temperature signal for compensating the variation in OLED efficiency over the full military temperature range, an OLED reference signal for controlling the cathode supply to the array, a second OLED reference for setting the proper gamma correction to the input data, and voltage and current reference levels for adjusting luminance over a >1000:1 range. An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components. The converter is an adjustable inverter that converts VDD to a negative supply used to bias the OLED via the COMMON input. Adjustment is managed by the control logic and registers.

Alternatively, VCOMMON can be externally provided by powering down the on-chip dc-dc converter and using external inputs.

The 2-wire serial interface is a slave only controller with a programmable address via an external pin (LSB). The interface provides access (read and write) to on chip registers. The registers allow the display to be configured for its various video modes and associated clock parameters. Additional functions include luminance control, display orientation, internal vs. external function selection, self-test mode and various sensor settings.

A system application block diagram for the WUXGA-R5 microdisplay is given in Figure 3.

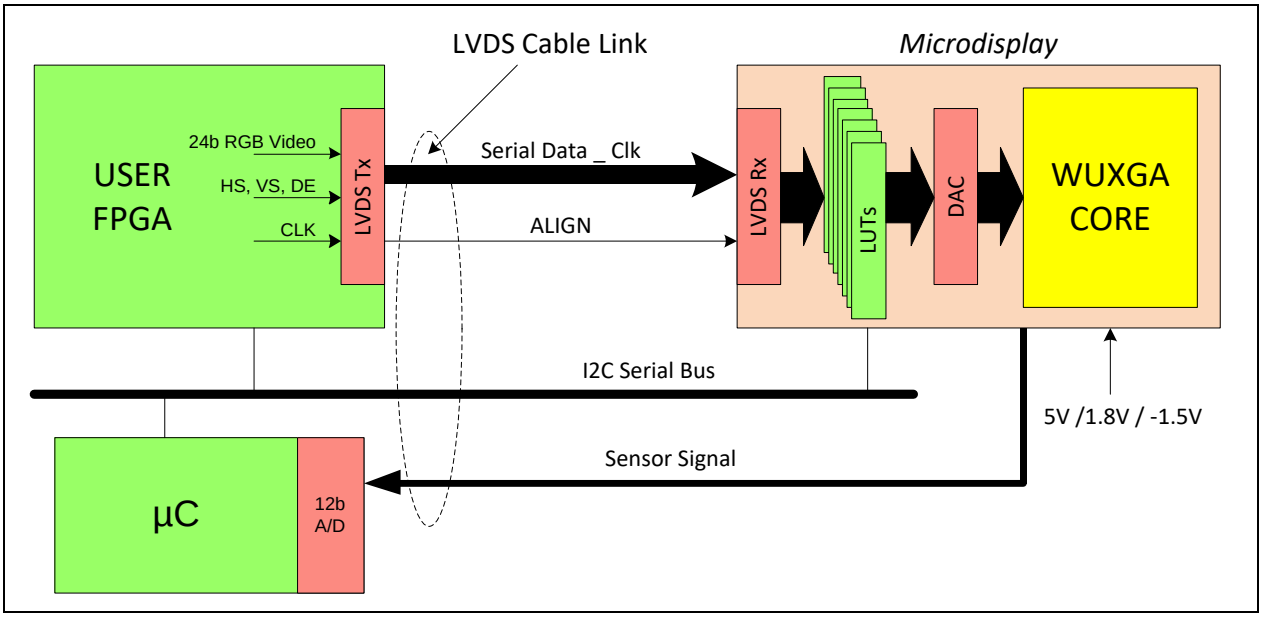


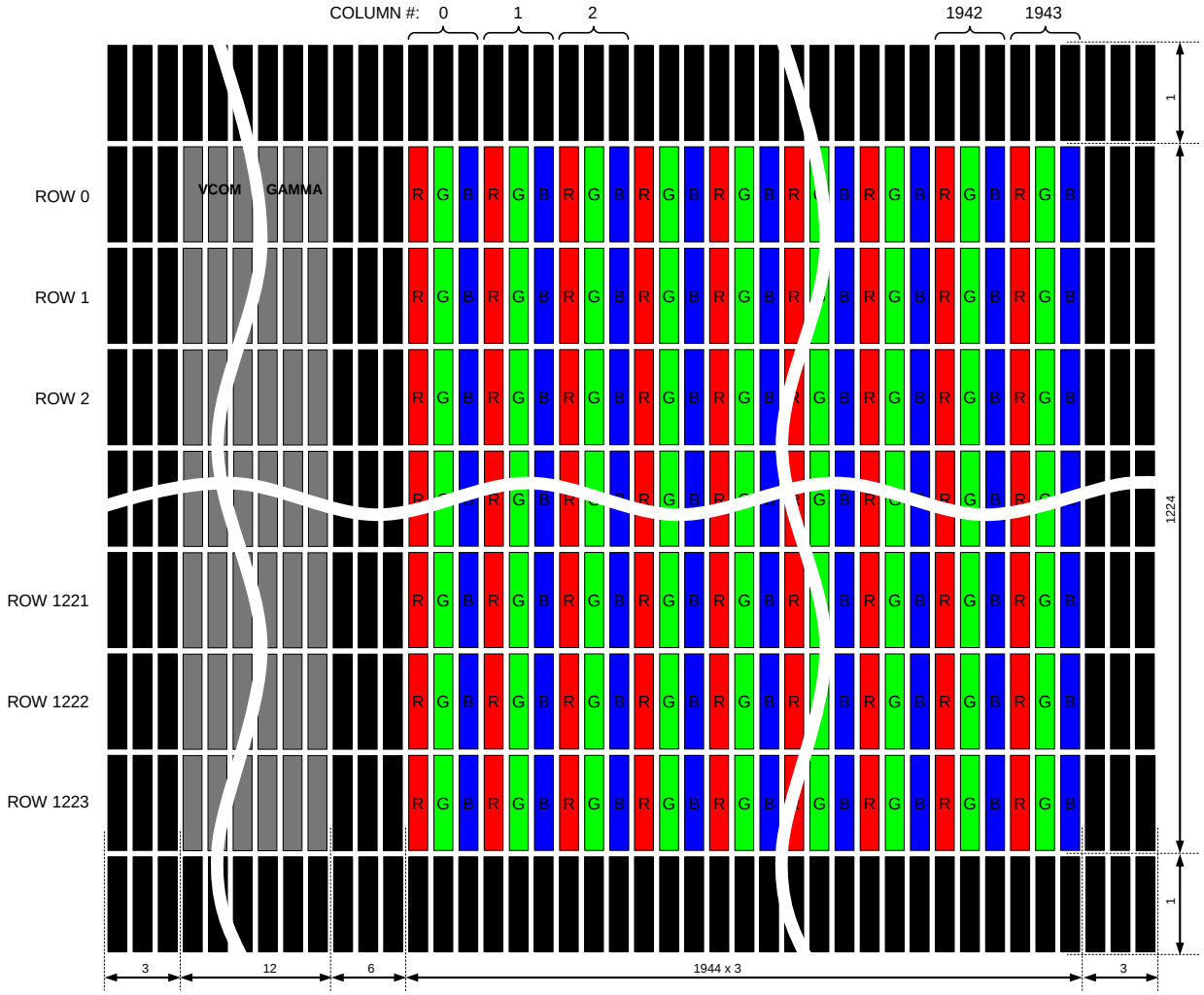
Figure 3: System application diagram

4. INPUT / OUTPUT DESCRIPTION

Pin #	Pin Name	Type	Description
1	GND	Power	Power return terminal.
2	GND	Power	Power return terminal.
3	RD3N	LVDS	LVDS Digital Data and Sync Input Port.
4	RD1P	LVDS	LVDS Digital Data and Sync Input Port.
5	RD3P	LVDS	LVDS Digital Data and Sync Input Port.
6	RD1N	LVDS	LVDS Digital Data and Sync Input Port.
7	GND	Power	Power return terminal.
8	SERADD	Logic In	Serial interface LSB address bit. Must be connected.
9	RD4N	LVDS	LVDS Digital Data and Sync Input Port.
10	RD0N	LVDS	LVDS Digital Data and Sync Input Port.
11	RD4P	LVDS	LVDS Digital Data and Sync Input Port.
12	RD0P	LVDS	LVDS Digital Data and Sync Input Port.
13	GND	Power	Power return terminal.
14	BURN_IN	Logic In	Activates Burn-In test mode. (active high, 1.8V CMOS)
15	RD5P	LVDS	LVDS Digital Data and Sync Input Port.
16	RD2N	LVDS	LVDS Digital Data and Sync Input Port.
17	RD5N	LVDS	LVDS Digital Data and Sync Input Port.
18	RD2P	LVDS	LVDS Digital Data and Sync Input Port.
19	VDD5	Power	Input power for the Display (5VDC). VAN
20	ENABLE	Logic In	Enable logic input.(used in Stereovision mode, 1.8V CMOS)
21	RD6P	LVDS	LVDS Digital Data and Sync Input Port.
22	RCKP	LVDS	LVDS source clock.
23	RD6N	LVDS	LVDS Digital Data and Sync Input Port.
24	RCKN	LVDS	LVDS source clock.
25	DAC OUT	Test	Used for monitoring the Ramp signal.
26	RESETB	Logic In	Asynchronous system reset (active low, 1.8V CMOS).
27	RAMP_TOP	Test	Test data output.
28	VPG	Power	Negative voltage bias for array protection switch. (-1.5 V)
29	RAMP_BOT	Test	Test data output.
30	VGN	Analog Out	Gamma sensor output signal. (0 to +2.5V)
31	TEST_OUT1	Test	Scan test output.
32	SDA	Logic I/O	Data port for the serial interface. Open collector output
33	TEST_OUT2	Test	Scan test input.
34	SCL	Logic In	Clock port for the serial interface. 400 KHz Max.
35	NC	Open	Open
36	LVDS_ALGN	Logic In	LVDS logic initialization signal (1.8V CMOS input).
37	NC	Open	Open
38	VDD1.8	Power	Input power for logic and I/O pads. (1.8VDC)
39	NC	Open	Open
40	VDD5_VCOM	Power	Input power for VCOM Generator. (DC2DC)

Shaded pins: Used for test purposes only, not for user application

5. PIXEL ARRAY LAYOUT



6. ELECTRICAL CHARACTERISTICS

Table 6-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	-0.3		2.5	VDC
VAN (VDD5)	Array Power Supply	-0.3		5.5	VDC
VDD5_VCOM	VCOM Converter Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3		0	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-45		+125	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 6-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	1.62	1.8	1.98	VDC
VAN(VDD5)	Array Power Supply	4.75	5	5.25	VDC
VDD5_VCOM	VCOM Converter Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
SDA, SCL	Serial Interface Supply	1.8		5	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-45	+25	+70	°C
Pdt	Power Consumption		350		mW

Table 6-3 : DC Characteristics

(Ta = 25°C, VDD =+1.8V, VAN = +5V, GND = 0V)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply		1.8		V
VAN/VDD5_VCOM	Array/VCOM Converter Power Supply		5		V
VCOM	Common electrode bias	-5	-2.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		0.6	V
Vih(1)	Digital input high level	1.2		VDD+0.3	V
Vol	Digital output low level		GND	0.5	V
Voh(1)	Digital output high level	VDD-0.2	VDD		V
Vlvds	LVDS input level	1		1.8	V
VGN	Gamma feedback signal	0		2.5	V
Ipix	Average Pixel Current per frame	0	4.3		nA
Ipix_inl	Average Pixel Current Integral Non Linearity				%
Ipix_dnl	Average Pixel Current Differential Non Linearity				%

(1) Except for the SDA and SCL lines which run up to +3.3 Volts

Table 6-4 : AC Characteristics – LVDS Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CM}	Common Mode Input Range		1.0	1.2	2.5	V
V_{IN}	Differential Input Voltage	V_{CM} = +1.2V	200	350		mV
I_{IN}	Input Current	V_{IN} = 1.8V			±10	µA
		V_{IN} = 1.0V			±10	µA
F_{TCLK}	LVDS Clock Frequency	WUXGA-R5 FR=85Hz			441.5	MHz
TT_{TCLK}	LVDS Clock Transition Time	F = 441.5MHz			0.68	ns
DC_{TCLK}	LVDS Clock Duty Cycle	F = 441.5MHz	45		55	%
SKWMG	Receiver Skew Margin with Deskew	F = 441.5MHz	200			ps

Table 6-5 : AC Characteristics – Other

(-45°C < Ta < +70°C, GND = 0V, VDD= +1.8V, VAN = +5.0V,
VCOM = -2V, VPG = -1.5V, 60 Hz refresh rate)

Symbol	Parameter	Min	Typ.	Max.	Unit
Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VAN	Average Van Power Consumption (VGA Mode 60 Hz refresh rate)		300		mW
Pd VDD	Average VDD Power Consumption (WUXGA-R5 Mode 60 Hz refresh rate)		8		mW
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode*		2.5		mW
Ta	Ambient Operating Temperature	-45		+65	°C

6.1 Timing Characteristics

6.1.1 Source Video Timing

The WUXGA-R5 backplane is configured to accept 2 pixels per clock. Source timing (Video timing prior to LVDS serialization) for single pixel per clock is provided for information only.

6.1.1.1 Single pixel per clock source timing

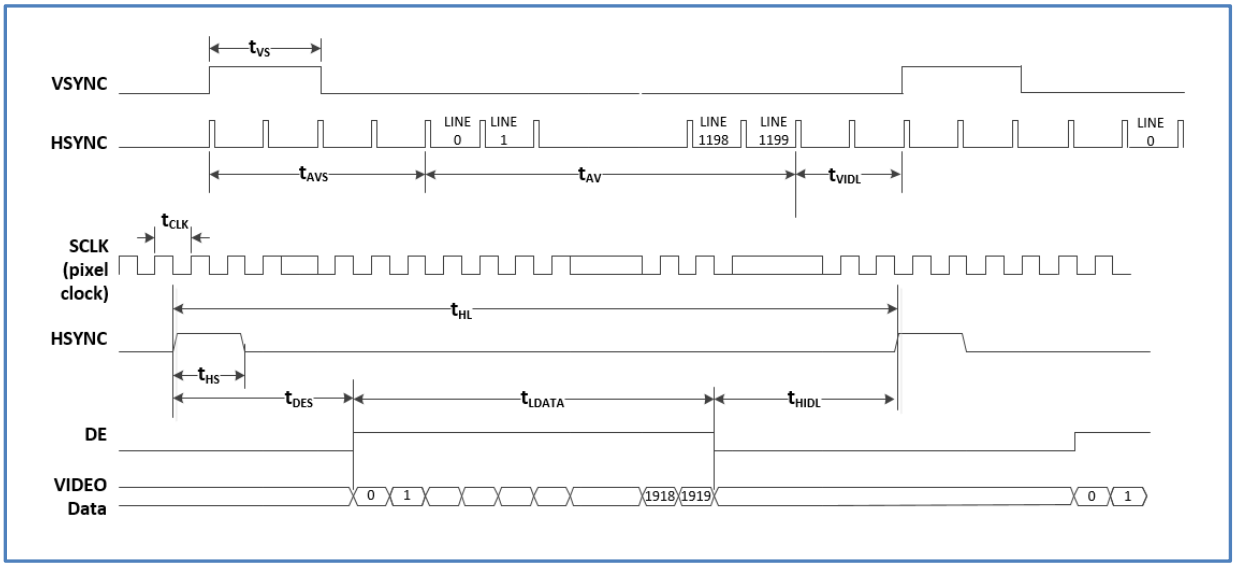


Table 6-6 : Video Input Timing Characteristics – 1 pixel per clock

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency Clock Period	f_{CLK}		154[1]		MHz
	t_{CLK}		6.49		ns
Clock Duty	D_{CLK}	45		55	%
VSYNC Pulse Width	t_{VS}	2		t_{AVS} - 1	Hsync period
Time to Active Video Start	t_{AVS}	t_{VS} + 2			Hsync period
Time to Next Vsync	t_{VIDL}	2			Hsync period
Active Video Lines	t_{AV}	714	1200	1224	Hsync period
HSYNC Pulse Width	t_{HS}	8		t_{DES} -8	SCLK period
Time to DE Start	t_{DES}	16			SCLK period
Time to Next Hsync	t_{HIDL}	8			SCLK period
Active Video Pixel	t_{LDATA}	1434	1920	1944	SCLK period

Note 1: WUXGA-R5@ 60Hz frame rate, Reduced Blanking Mode, 1 pixel per clock

6.1.1.2 Dual pixel per clock source timing

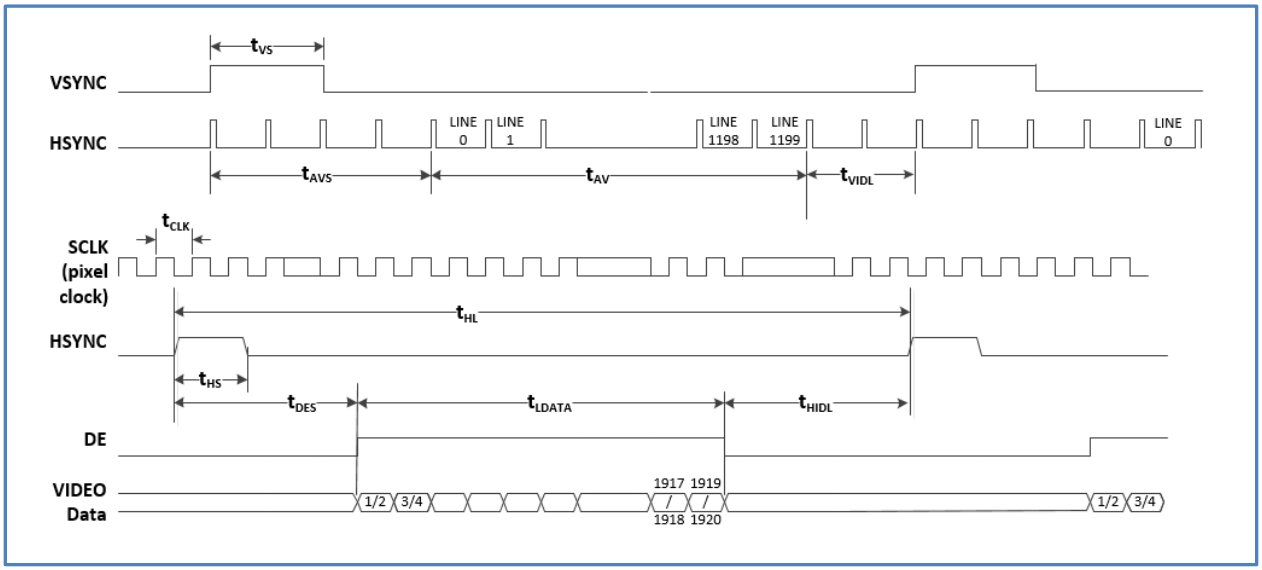


Table 6-7 : Video Input Timing Characteristics – 2 pixels per clock

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency Clock Period	f_{CLK}		77[1]		MHz
	t_{CLK}		198		ns
Clock Duty	D_{CLK}	45		55	%
VSYNC Pulse Width	t_{VS}	2		t_{AVS} - 1	Hsync period
Time to Active Video Start	t_{AVS}	t_{VS} + 2			Hsync period
Time to Next Vsync	t_{VIDL}	2			Hsync period
Active Video Lines	t_{AV}	714	1200	1224	Hsync period
HSYNC Pulse Width	t_{HS}	8		t_{DES} -8	SCLK period
Time to DE Start	t_{DES}	16			SCLK period
Time to Next Hsync	t_{HIDL}	8			SCLK period
Active Video Pixel	t_{LDATA}	717	960	972	SCLK period

Note 1: WUXGA-R5@ 60Hz frame rate, Reduced Blanking Mode, 2 pixels per clock

6.1.2 Gamma Sensor Timing Diagram

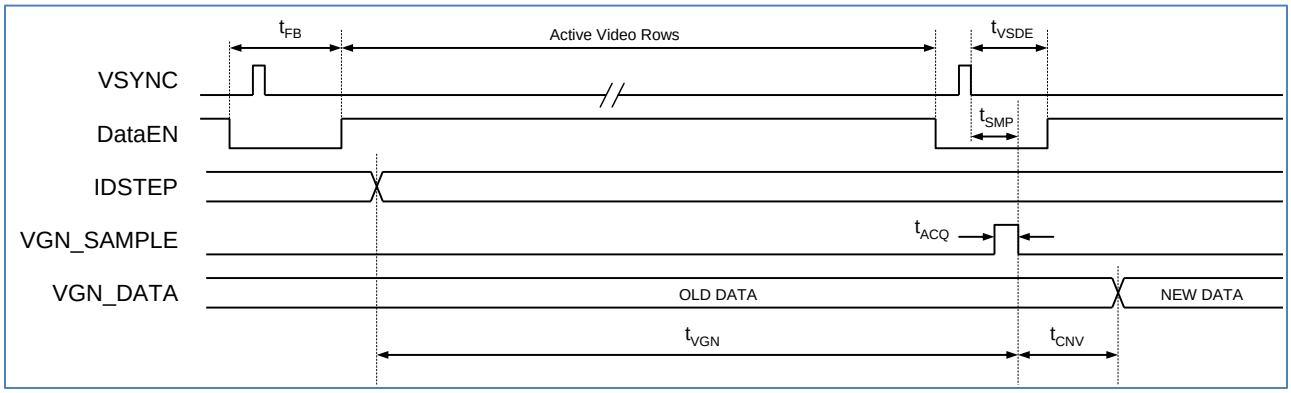


Table 6-8 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	1			%
VGN Sampling Time	t_{SMP}	t_{ACQ}		t_{VSDE}	
A/D Acquisition Time	t_{ACQ}	20			µs
A/D Conversion Time	t_{CNV}				

7. OPTICAL CHARACTERISTICS

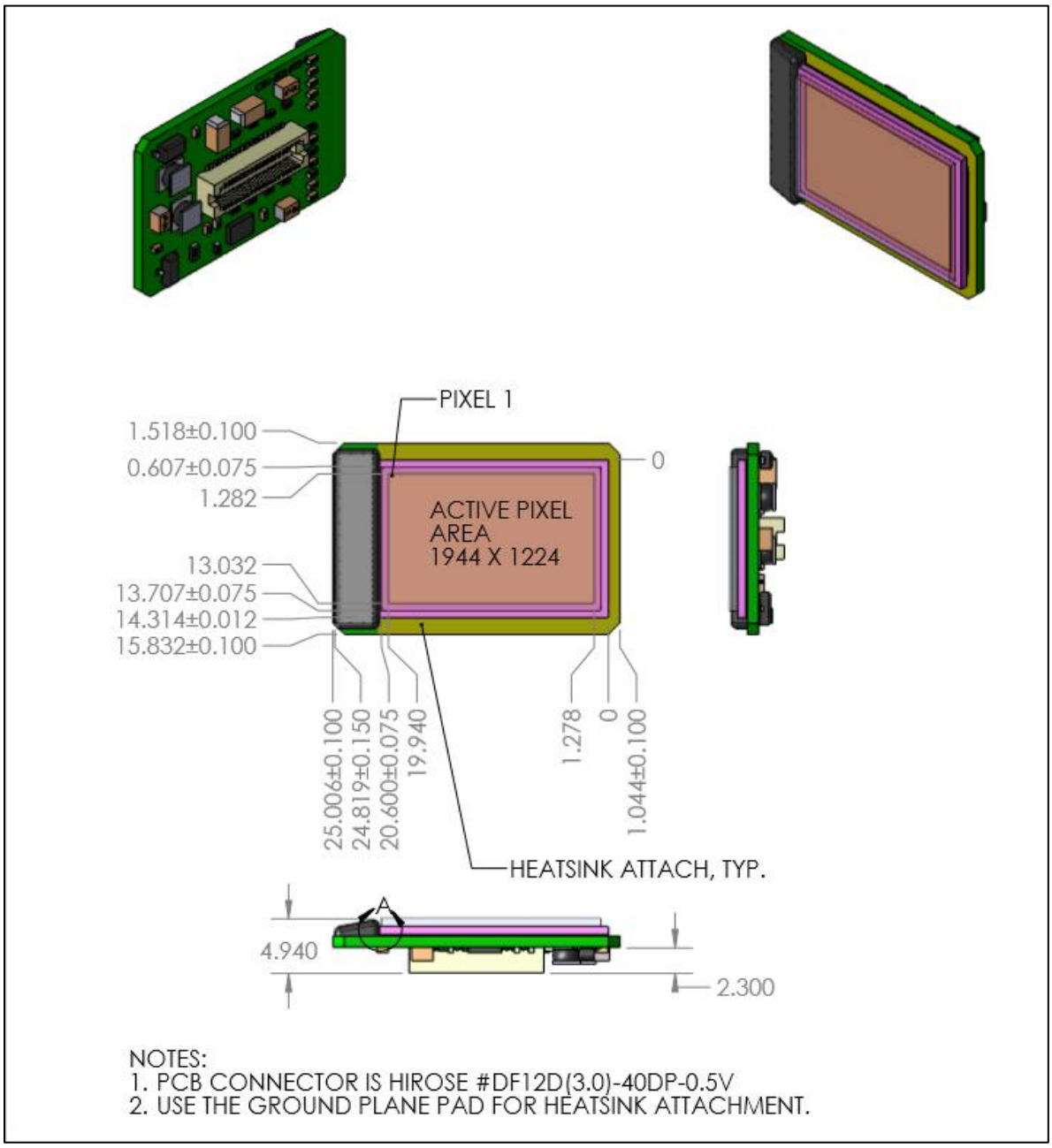
Table 7-1 : WUXGA-R5 XL Color Microdisplay Optical Characteristics

Conditions: Ta = +20ºC, VDD = +1.8V, VAN = +5V, VPG = -1.5V, VCOM = internally generated

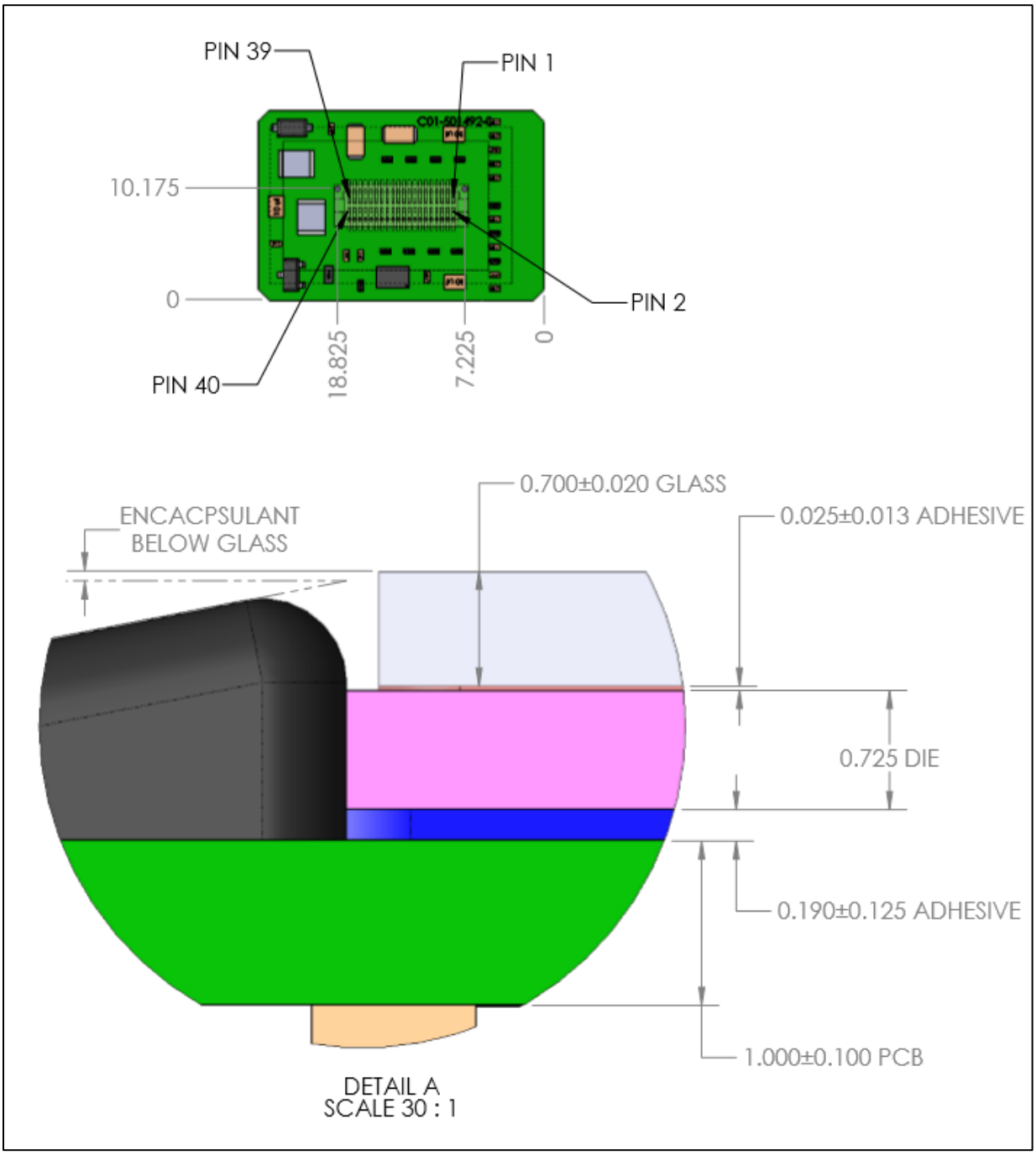
Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level	0.35	140	400	cd/m^2
	Variability	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE White	CIE-X	0.270	0.320	0.340	
	CIE-Y	0.320	0.350	0.380	
CIE Red	CIE-X	0.570	0.620	-	
	CIE-Y	0.320	0.350	0.360	
CIE Green	CIE-X	0.210	0.300	0.33	
	CIE-Y	0.450	0.510	-	
CIE Blue	CIE-X	-	0.141	0.190	
	CIE-Y	-	0.117	0.170	
GL	Gray Levels Per Color	256		1024	levels
F_R	Refresh Rate	30		85	Hz
FF	Emissive Area/Total Sub-pixel Area		0.69		
U_{LA}	End to end large-area uniformity	85(1)			%
S_{VH}	Pixel spatial noise at typical luminance (1STD)			5	%
S_{LOT}	Peak-to-peak luminance variation over operating temperature range			8(2)	%
T_{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: At 100% of gray level brightness and150 cd/m2 luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

8. MECHANICAL CHARACTERISTICS



Front View



Rear View Detail

Connector J1

Manufacturer:	Hirose
Manufacturer Part Number:	DF12D(3.0)-40DP-0.5V

Mating Connector Information

Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-40DS-0.5V

Weight:	< 3 grams

Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.3 mm (both axes)

The WUXGA-R5 package provides a means for improved thermal management of the microdisplay. The silicon die is bonded directly to a grounded copper layer on the top-side of the carrier board. The gold-plated copper layer is exposed on three sides and can be mounted against a heat sink for efficient heat removal.

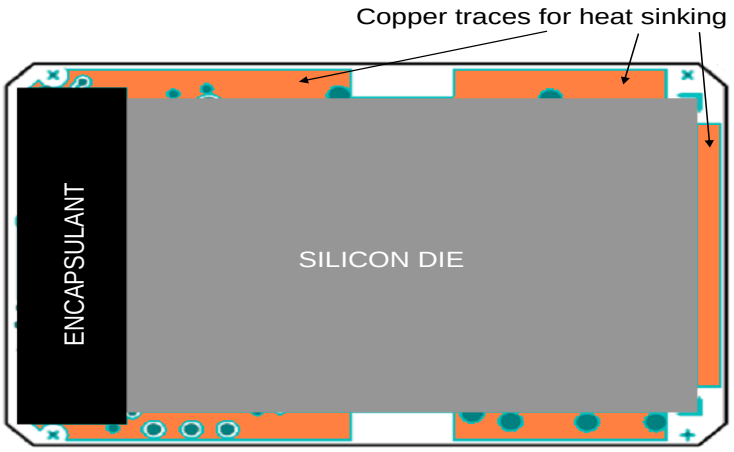
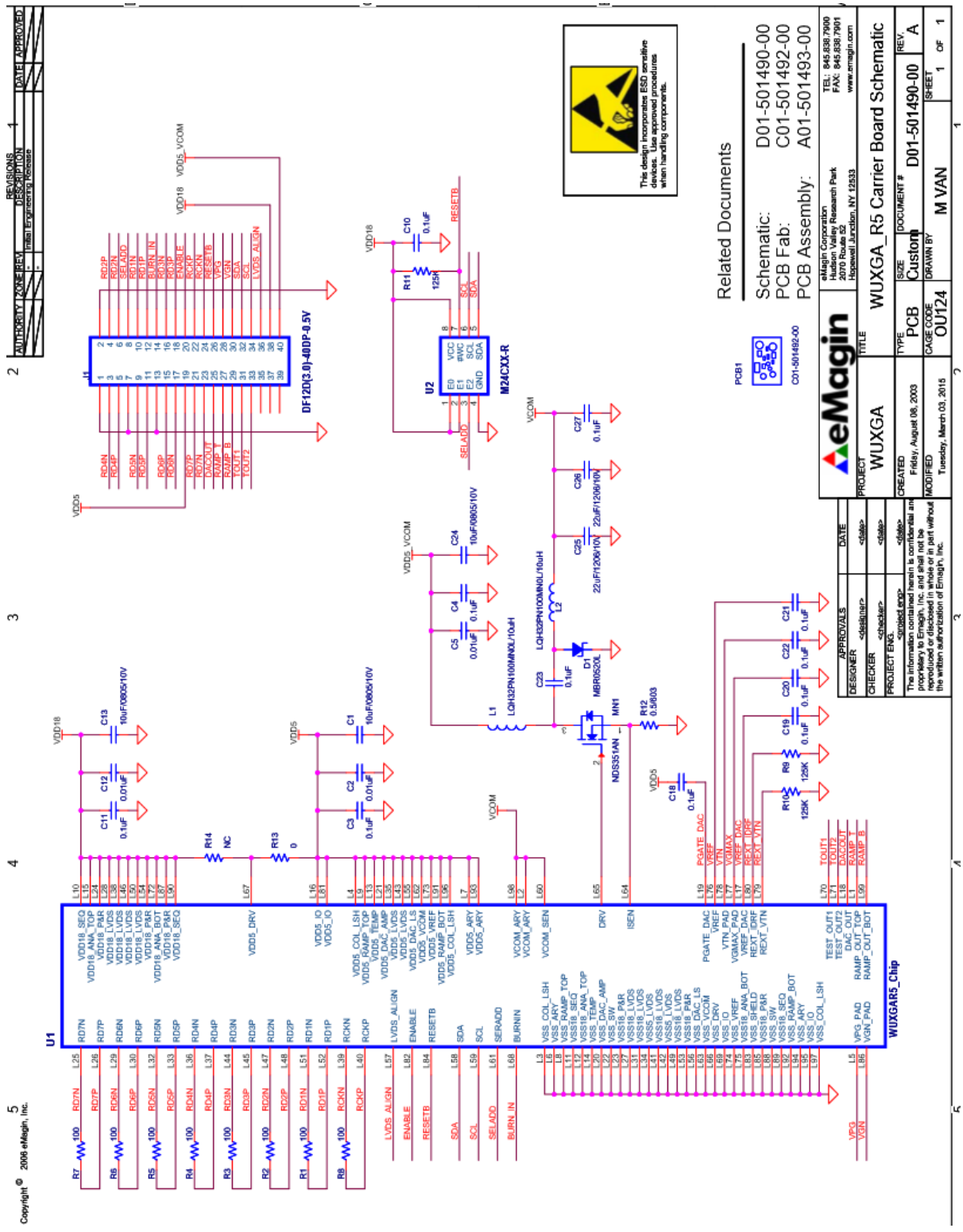


Figure 4: Display-side view of WUXGA-R5 microdisplay

9. CARRIER BOARD SCHEMATIC (D01-501490-00 REV A)



10. DETAILED FUNCTIONAL DESCRIPTION

10.1 Video Interface

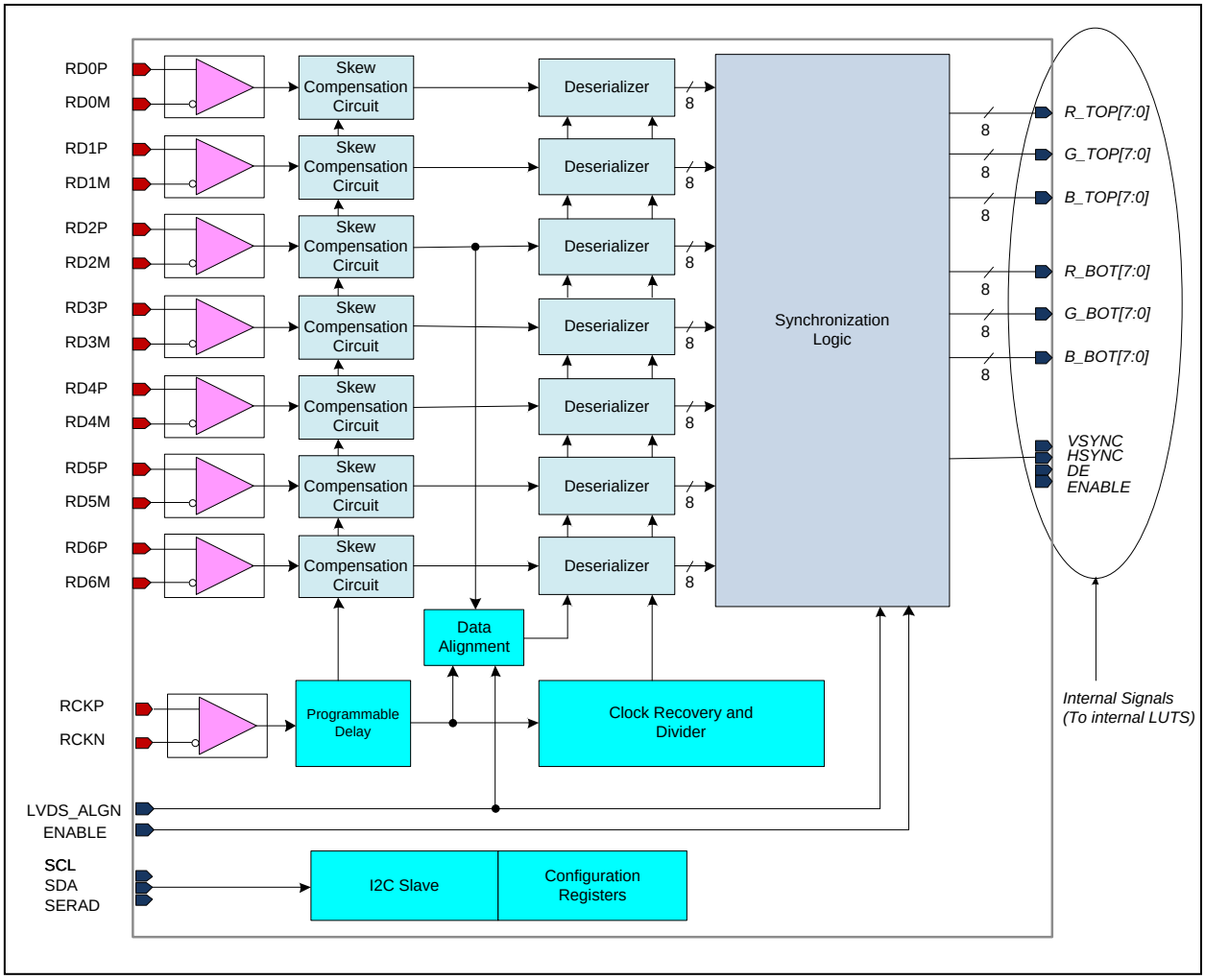


Figure 5: LVDS Receiver Block Diagram

The video interface is comprised of 7 data signal pairs and 1 clock signal pair, which are low voltage differential signaling (LVDS), and one control signal (LVDS_ALIGN) which is a CMOS signal. It is different from the industry standard LVDS interface format. The receiver input PADs expect a standard LVDS output signaling, but the serialization and protocol is different. The LVDS data pairs should be 8-

bit serialized data instead of 7-bit serialization. The LVDS clock also should be a serialized signal in the same way as the data channel with a toggle pattern instead of PLL clock. It always should be a 4 times multiple of the pixel clock. The LVDS receiver uses both edges of the clock and it has a special skew compensation circuit to compensate the skews among the 7 data pairs and the data alignment logic. So, the LVDS receiver expects the special skew compensation patterns through all LVDS channels including the clock channel when the power is first applied and the alignment patterns to identify the MSB of the 8 bits serial data at every VSYNC at least. (Ref. to Appendix B)
The WUXGA R5 LVDS interface is designed to receive 2 pixels per clock (2 x 24-bit RGB data). Refer to Table 4 for the LVDS port mapping.

Table 10: Supported Video Formats

	Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
Reduced Blank	WUXGA	H	106.13 KHz	2080	1920	48	32	80
	1920X1200	V	84.97 Hz	1249	1200	3	6	40
	85Hz	P	220.75 MHz					
	UXGA	H	106.11 KHz	1760	1600	48	32	80
	1600X1200	V	84.95 Hz	1249	1200	3	4	42
	85Hz	P	186.75 MHz					
	FHD1080P	H	95.43 KHz	2080	1920	48	32	80
	1920X1080	V	84.90 Hz	1124	1080	3	5	36
	85Hz	P	198.50 MHz					
VESA Standard	WUXGA	H	74.56 KHz	2592	1920	136	200	336
	1920X1200	V	59.88 Hz	1245	1200	3	6	36
	60Hz	P	193.25 MHz					
	UXGA	H	74.54 KHz	2160	1600	112	168	280
	1600X1200	V	59.87 Hz	1245	1200	3	4	38
	60Hz	P	161.00 MHz					
	FHD1080P	H	67.16 KHz	2576	1920	128	200	328
	1920X1080	V	59.96 Hz	1120	1080	3	5	32
	60Hz	P	173.00 MHz					

Table 11: Example LVDS Interface Timing

Reduced Blank Video	Video Format			LVDS Interface Timing			
	Pixel/Line	Line/Frame	Pixel Clock MHz	LVDS Format (pairs) X (serial)	No. of Pins (pairs w. clock)	LVDS Data rate Mbps	LVDS Clock MHz
WUXGA (85Hz) 1920X1200	2080	1249	220.75	7 X 8	8	883.00	441.50
1080P (85Hz) 1920X1080	2080	1124	198.50	7 X 8	8	794.00	397.00
UXGA (85Hz) 1600X1200	1760	1249	186.75	7 X 8	8	747.00	373.50

Table 4 LVDS Port Mappping

LVDS Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD6P/RD6N	B5_EV	B4_EV	B3_EV	B1_EV	B0_EV	B2_EV	G7_EV	R0_EV
RD5P/RD5N	G6_EV	G5_EV	G1_EV	G0_EV	G4_EV	G3_EV	G2_EV	B7_EV
RD4P/RD4N	R7_EV	R1_EV	R6_EV	R5_EV	R4_EV	R3_EV	R2_EV	B6_EV
RD3P/RD3N	-	DE	-	VSYNC	-	HSYNC	-	ENABLE
RD2P/RD2N	B5_OD	B4_OD	B3_OD	B1_OD	B0_OD	B2_OD	G7_OD	R0_OD
RD1P/RD1N	G6_OD	G5_OD	G1_OD	G0_OD	G4_OD	G3_OD	G2_OD	B7_OD
RD0P/RD0N	R7_OD	R1_OD	R6_OD	R5_OD	R4_OD	R3_OD	R2_OD	B6_OD

10.2 OLED Gamma Correction

Due to the non-linear electro-optic characteristic of the OLED pixel, a gamma correction signal must be applied to the video input signal to achieve a linear response at the display output. Since the optimum gamma curve will vary with temperature and luminance, it should also be regularly updated to account for changes in operating conditions. The display chip includes a LUT for each of the 3 color data paths consisting of 256 10-bit words. Each 8-bit input data value is converted to the appropriate 10-bit gamma corrected output value via the LUT. An extra LUT is included on-chip to buffer the externally generated LUT values that are provided via the serial port, and enables a fast update of the data path LUTs during

the frame overscan time. Each of the RGB LUTs can be programmed individually to control the color balance of the display.

The LUT values are generated by an external micro-controller using the VGN sensor information provided by the display chip as described in section 10.5.5. An example of a typical input transfer curve that was generated as a piecewise-linear function using a 9-entry table (Q0-Q8) is shown in Figure 6. The 8-bit source video byte is converted to a 10-bit word for input to the pixel driver. Intermediate data points are extrapolated linearly from the nearest table entries.

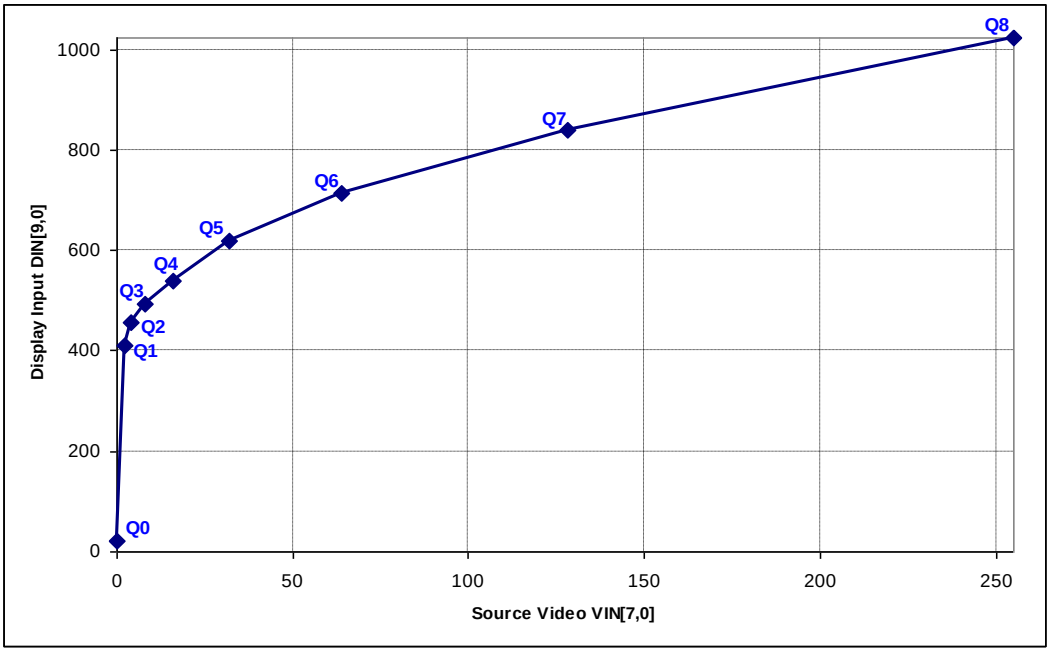


Figure 6: Typical input transfer function for linearized optical response

10.3 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

A block diagram of one column drive circuit is shown in Figure 7. The 1944 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into

the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

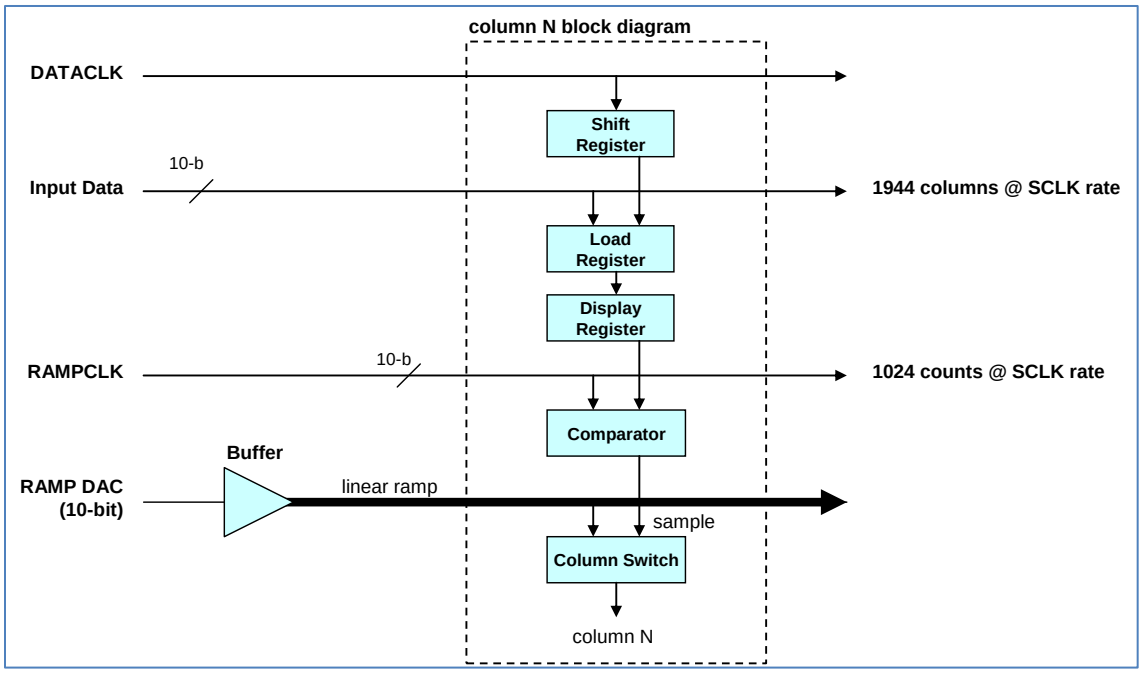


Figure 7 : Data sampling for Column N

A timing diagram for the data sampling process is shown in Figure 8. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VAN rail after 1024 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via register bits RAMPDLY, its peak value can be set using register VDACMX, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

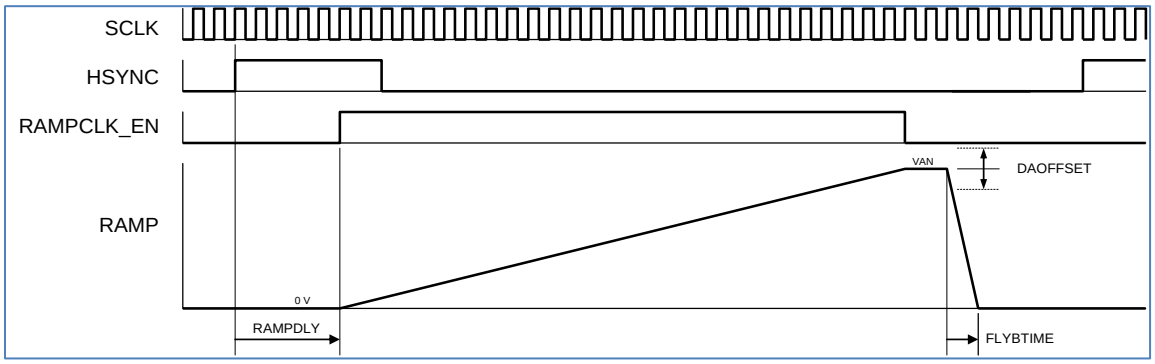


Figure 8 : Timing diagram for column data sampling

10.4 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, LFTPOS, RGTPOS, TOPPOS and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before a video image is displayed.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

10.4.1 Vertical Position Control

To support the vertical positioning of the display within the extra 24 pixels provided on each column of the array, an on-chip shift register function is provided in the Row sequencer logic, and controlled by registers TOPPOS and BOTPOS. The starting row for the active video is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in WUXGA mode is vertically centered in the array. The Vertical positioning logic will blank rows at the beginning and end of each frame of data to allow a vertical image shift of up to 24 pixels in steps of 1 or 2 pixels in WUXGA mode.

10.4.2 Horizontal Position Control

To support the horizontal positioning of the display within the extra 24 pixel provided on each row of the array, an on-chip shift register function is provided after the LUT block, and controlled by registers LFTPOS and RGTPOS. The Horizontal Shifter adds black pixel data to the beginning and end of each line of data to allow a horizontal image shift of up to 24 pixels in steps of 1 pixel in WUXGA mode.

10.4.3 Interlaced Modes

Bits SCMODE in the DISPMODE register are used to select either progressive (default) or interlaced modes.

Field status in interlaced mode is provided via the ENABLE input pin. The state of this pin is latched on the falling edge of VSYNC. When register bit SET_FIELD = “0” then a logic low at the ENABLE pin indicates that Field 1 (odd field) is active, and a logic high indicates that Field 2 (even field) is active. The opposite states are indicated when SET_FIELD is set to 1.

10.4.4 Stereovision Mode

The WUXGA-R5 is designed with binocular stereovision applications in mind. As a result of the fast OLED response time and the presence of a storage capacitor at each pixel, it has been verified that the microdisplay can operate at low refresh rates without showing flicker.

This allows the displays to be used with a frame or field sequential (more generally known as time sequential) stereovision mode using a single video input channel, and therefore providing a simple means to leverage the capabilities of PC compatible computers using stereo compatible graphics adapters, such as the Nvidia GeForce series. The frame sequential stereovision mode supported should follow the Video Electronics Standards Association (VESA) Connector and Signal Standards for Stereoscopic Display Hardware. This standard is available from VESA at www.vesa.org.

The ENABLE input pin allows for a direct implementation of the VESA standard without additional external components. The microdisplay can be programmed for either an active high or low Enable, allowing a single signal to be used with two displays. In such a configuration, one display scans and displays while the other one holds and displays.

The ENABLE input acts, when set low, as a mask for HSYNC and VSYNC. It does not blank the display but prevents it from acquiring another frame of data until released. This is a real time input. The active state (high or low logic level) is programmed by the SET_ENABLE bit in the VINMODE resister.

The 3D-MODE bit of the DISPMODE register will be used to set either Time Sequential mode to activate the stereovision mode of operation (1) or Normal (non-3D) operation (0).

Frame Sequential Mode:
In Time Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bits in the DISPMODE register are set to Progressive Scan Mode (00H) for frame sequential mode. The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard mentioned above, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The stereovision mode is controlled by both the Enable input pin and by the SET_ENABLE bit of the VINMODE register. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0"). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display must be configured with Enable active high (SET_ENABLE="1"). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

Field Sequential Mode:
In Field Sequential Mode each video field in an interlaced image contains information for either the left or right eye. Consequently, the resolution is reduced in half for each display.

When 3D-MODE="1" the SCMODE bits in the DISPMODE register are set to either Interlaced or Pseudo Interlaced Mode to activate field sequential mode. The operation of the Enable input pin and the SET_ENABLE bit will be similar to Frame Sequential Mode except that now the Enable input toggles at the field rate. The polarity of the field corresponding to the active state of the ENABLE input will be set by the SET_FIELD bit in the VINMODE register. When SET_FIELD="0" the odd field is applied during the active state for ENABLE, and the even field is assumed during the active state for ENABLE when SET_FIELD="1".

For standard WUXGA-R5 operation, the SET_ENABLE bit needs to be set to 0 (logic low), which is the power-on default value, and the Enable pin input needs to be tied to Ground.

10.4.5 Row Duty Rate Control

The duty rate for a row of data is defined as the fraction of a frame period during which the pixels maintain a programmed value; for the remainder of the frame period the pixels will be driven to black.

A Row Reset function is provided in the WUXGA-R5 to allow the duty rate of rows to be controlled between 0 and 100% (default condition). The register ROWRESET[9,0] is used to set the number of Hsync cycles during which the pixel data is driven to black during a frame period. For ROWRESET=0

the pixel data is never driven to black and the duty rate for pixel data is equal to 100% (default). For ROWRESET=W the pixels in any row are driven to black for the final 2*W Hsync cycles in an active frame period.

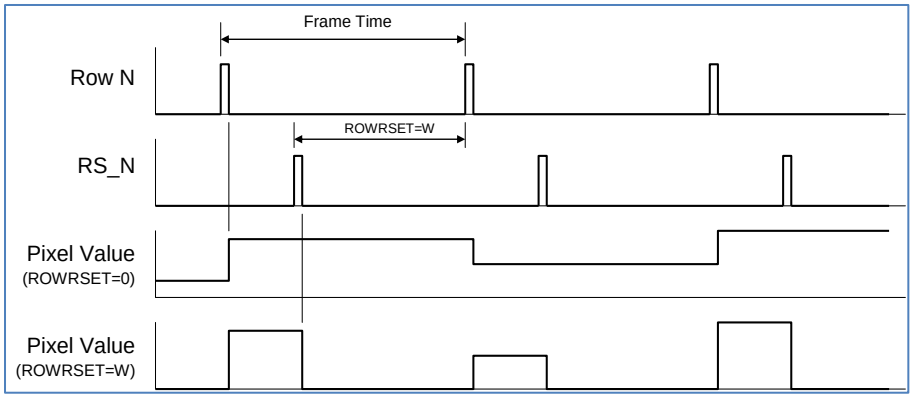


Figure 9 : Timing diagram showing Row Reset functionality.

The operation of the Row Reset function is depicted in the timing diagram shown in Figure 9. All the pixels contained in ROW N are programmed during the Nth horizontal line scan following the initialization line scans which occur at the beginning of a video frame. Normally this pixel data is stored in the pixel and remains unchanged until it is refreshed during the next frame period. When the Row Reset function is activated, the pulse RS_N is generated at a position determined by the value of register ROWRESET. For example, when the register value is equal to W the rising edge of RS_N occurs exactly 2*W Hsync cycles prior to the next programming cycle for ROW N. The pulse RS_N sets all the pixels in ROW N to black until the next programming cycle. All rows in the array will operate at the same duty rate. As a result the duty rate for all the rows in the pixel array will be given by

$$ROW\_DUTY = \frac{2 * W * T_{HSYNC}}{T_{FRAME}}$$

10.5 Sensor Functions

10.5.1 Temperature Readout

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register ANGPWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

10.5.2 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VAN supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.

Register VDACMX[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting has been determined by measurement to be 78h for normal operating conditions. Refer to section 11.12 for more detail.

10.5.3 Pixel Bias Sensor

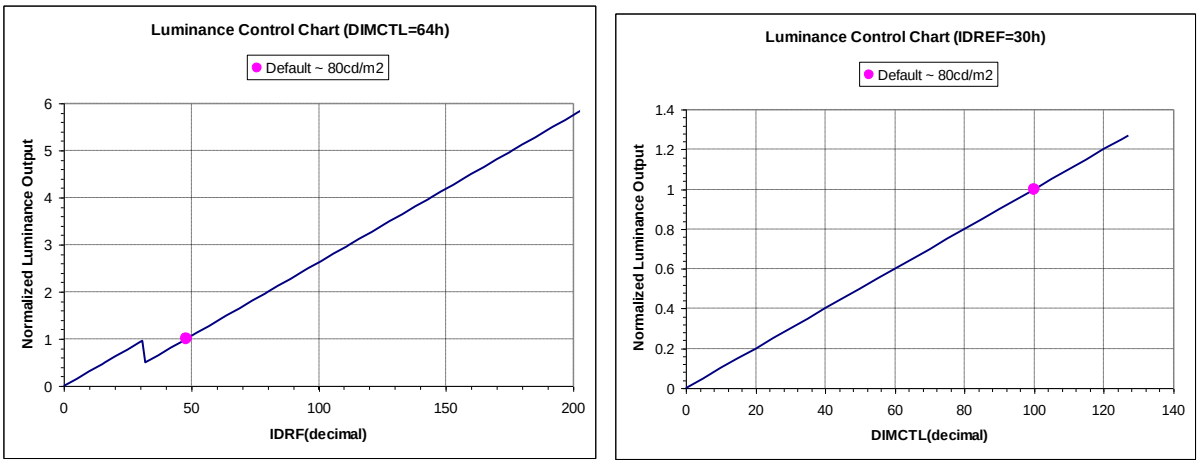
Register BIASN[2,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to ~10mW increase of power consumption for the array under normal operating conditions. It is recommended to use the BIASN=3 setting for best performance.

10.5.4 Luminance Control (Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is effected by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRF. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRF_COARSE in register IDRF provide a coarse adjustment of the maximum luminance level, while the IDRF_FINE bits enable the coarse level to be fine-tuned. Figure 10 shows the ideal luminance output at gray level = 255 in a color display for various settings of the IDRF and DIMCTL registers.

The maximum IDRF value is 0xDF. Going beyond is equivalent to rolling over to 0x00
The user should note that eMagin Corporation recommends keeping the IDRF value below 0XC0 to reduce significant increases in power consumption and operating temperature that will reduce the microdisplay lifetime.
Practical values for typical operation should not exceed 0x70 for the WUXGA-R5 Color XL Microdisplay.



(a) (b)

Figure 10 : Typical maximum luminance for various IDRF (a) and DIMCTL (b) settings

Large step changes in either the IDRF or DIMCTL register values are not recommended as they may result in unstable dimming control and high component stresses, particularly at ambient temperatures below 0°C. The recommended procedure for increasing luminance is to increment either of the control registers by only 1h per I^2C write instruction until the desired final luminance is reached. For example, to increase IDRF from 30h to 50h would require a sequence of 32 write instructions.

10.5.5 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a linear optical response from the WUXGA-R5 display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The WUXGA-R5 display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value $\boldsymbol{VGN_i}$, corresponding to one of 8 internally fixed grayscale levels $\boldsymbol{GL_i}$, is selected by setting bit IDSTEP in register GAMMASET via the serial port. The VGN signal is internally fixed for a full-scale output range of VAN/2. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDSTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word ***DVGN$_i$[9,0]*** using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

where ***VGN$_{MAX}$*** is either VAN or VAN/2 as determined by bit VGNSEL. Each of these data values must be further multiplied by a correction factor ***CF$_i$*** to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

where the empirically determined values for factor ***CF$_i$*** are given in Table 10-13.

Table 10-13: Correction Factor values

CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.870	0.880	0.900	0.922	0.940	0.955	0.968	1

Using the derived values for ***GC$_i$*** and their corresponding grayscale coordinates ***GL$_i$***, the 8-entry Gamma Correction table consisting of data points ***Q$_i$*** = (***GL$_i$***, ***GC$_i$***) can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 10-14.

Table 10-14: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
IDSTEP[0]	0h	1h	2h	3h	4h	5h	6h	7h
VGN$_i$ (volt)	1.839	1.876	1.913	1.964	2.045	2.159	2.318	2.500
GC$_i$ (dec)	662	698	727	766	814	872	941	1023
GL$_i$ (dec)	2	4	8	16	32	64	128	255

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in Figure 11. The input to the LUT for each color of the video source is represented by the 8-bit signal VIN[7,0], and the output of the LUT (which is also the input to the microdisplay) is represented by the 10-bit signal DIN[9,0]. For example, the Y coordinate for the intermediate point Q(x, y) on the line segment formed between the gamma table points Q6 and Q7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations before loading it into the data-path LUTs in the microdisplay. A buffer LUT is used in the microdisplay to temporarily store the data as it is transferred from the microcontroller via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

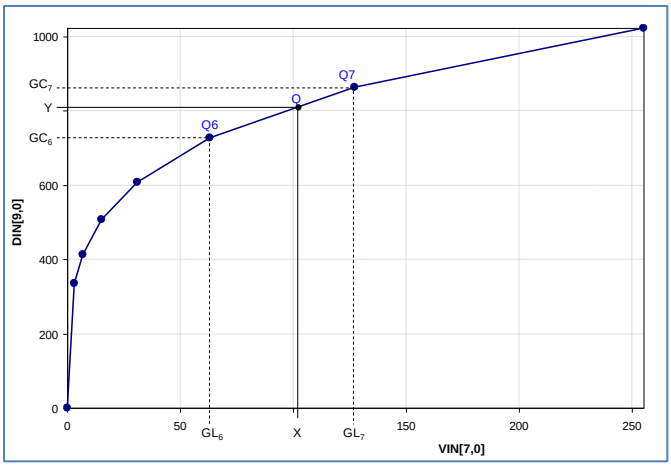


Figure 11 : Generating intermediate points by linear interpolation

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 12 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the WUXGA-R5 design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

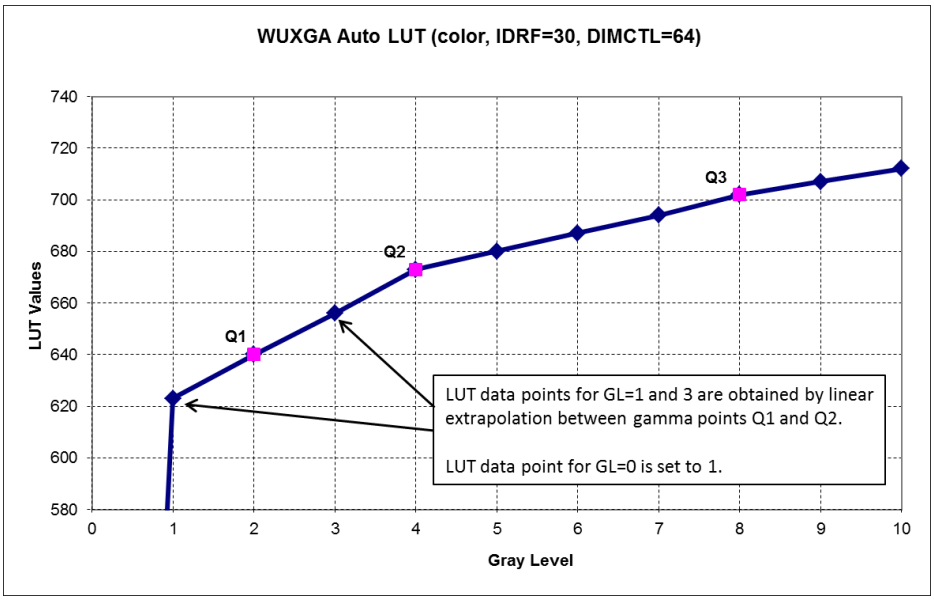


Figure 12 : Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^{\gamma}$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^{\gamma} = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^{\gamma} * 1023$$

For the case of a linear optical response (γ=1) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the System Gamma parameter are shown in Figure 13 and the corresponding system response curves for the display are given in Figure 14.

The System Gamma function is implemented in the DRK Firmware and is accessible to the user in the DRK UI Software. Contact eMagin for the latest DRK FW and SW.

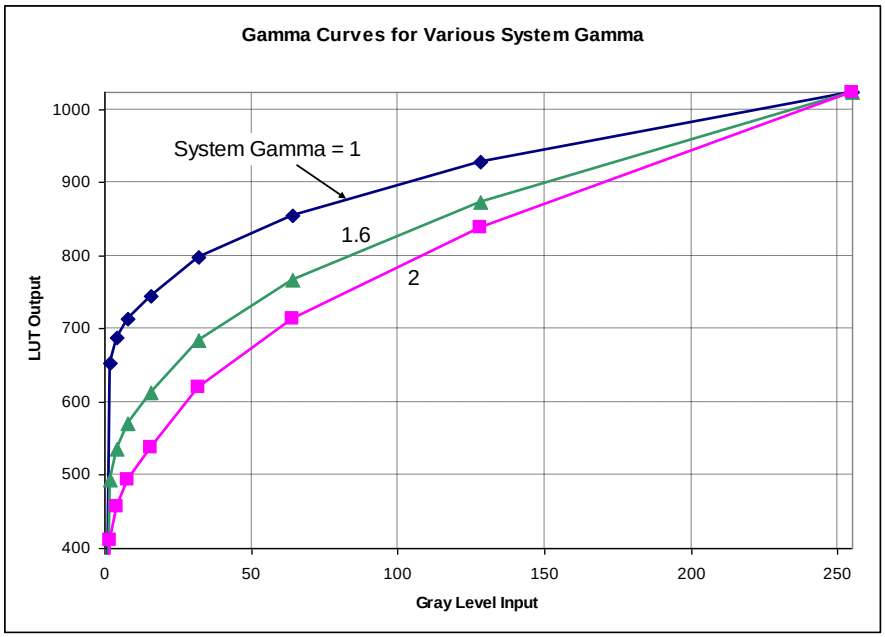


Figure 13 : Gamma curves for arbitrary System Gamma

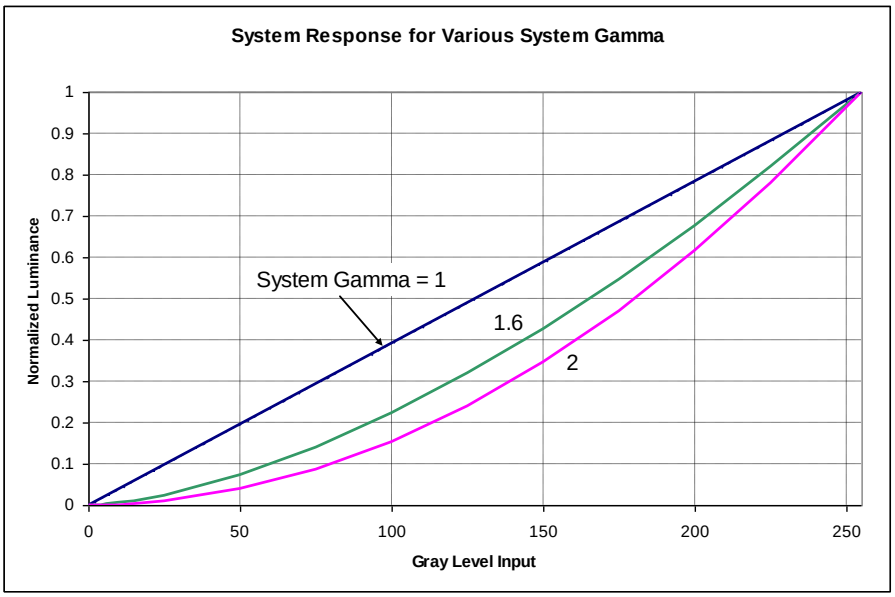


Figure 14 : Display system response for arbitrary system gamma

10.6 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0], VCOMCTL[7,0] and VCOMMODE[3,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A block level schematic of the Cuk converter that is employed in the WUXGA-R5 application is shown in Figure 15.

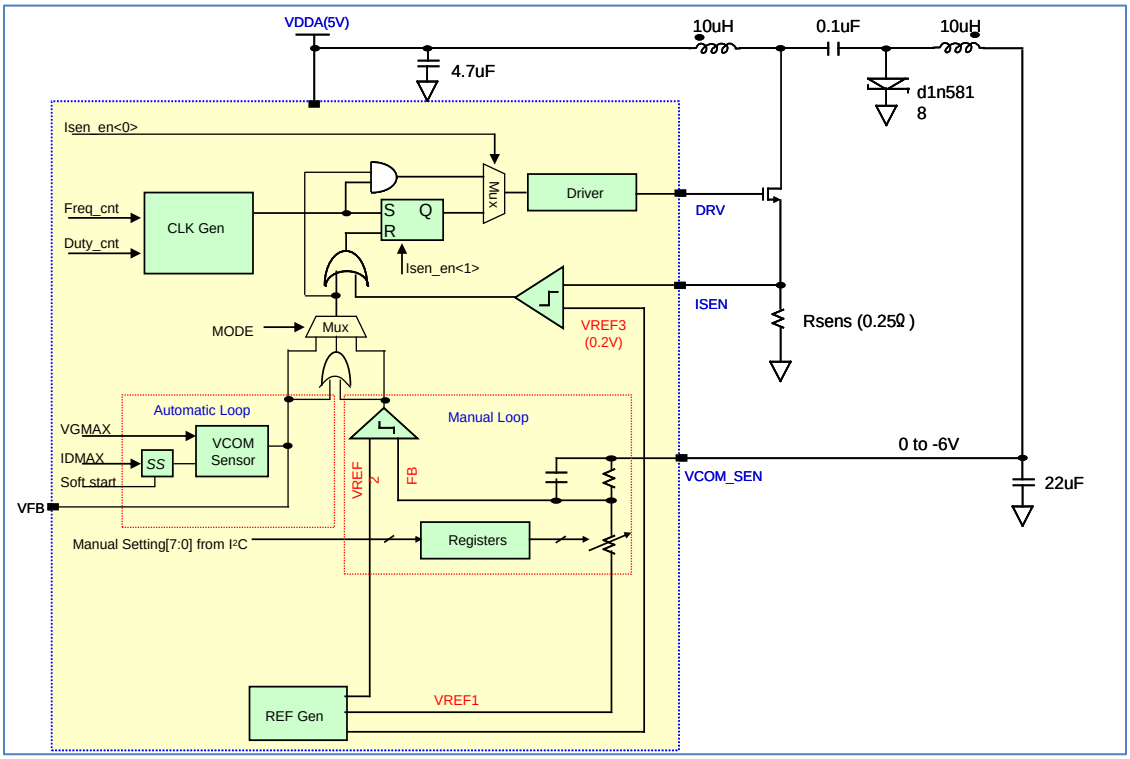


Figure 15 : Schematic of DC-DC controller function

Two modes of operation, selected via register VCOMMODE, are provided for the controller function. Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically

regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the dimming and luminance regulation functions via IDRF and DIMCTL are not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.

10.7 Serial Interface

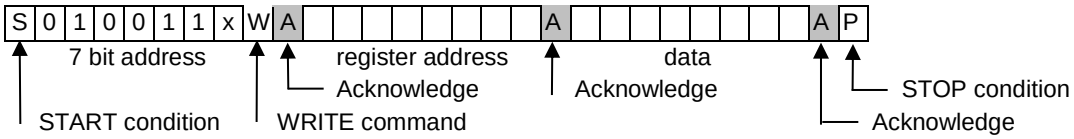
The serial interface consists of a serial controller and registers. The serial controller follows the I2C protocol. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

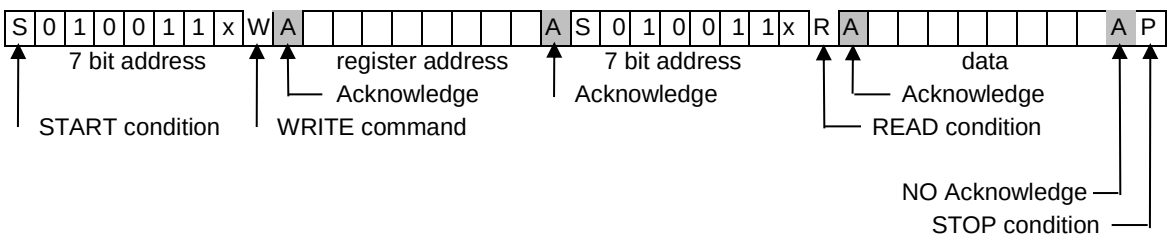
The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010011X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 10-15.

Write Mode: Address is 6C (or 6E if SERADD = 1)

Read Mode: Address is 6D (or 6F is SERADD =1)

Sequential Read/Write Operation
The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

It is possible to run the I^2C interface without source clock or any sync signals.

Interface maximum frequency: 400 KHz.

Table 10-15 : I2C Address Summary

WUXGA		0	1	0	0	1	1	SA	w/r	
SA = 0	write:	0	1	0	0	1	1	0	0	= 0x 4C
	read:	0	1	0	0	1	1	0	1	= 0x 4D
SA = 1	write:	0	1	0	0	1	1	1	0	= 0x 4E
	read:	0	1	0	0	1	1	1	1	= 0x 4F

10.8 Power-On Sequence

To ensure proper startup and stabilization of the display the following power-on sequence is recommended:

1. Turn on VDD, VAN, and VPG supplies (these can be simultaneous)
2. A ramp-up time of 0.2 to 20ms for VAN and VDD is recommended for best performance
3. The ramp-up time for VPG is not critical and it can be turned on anytime
4. Configure the display registers to the desired startup state
5. Turn on the display by setting the DISPOFF bit in register DISPMODE to “0”

Figure 16 shows the timing diagram for the power supplies and control signals during startup when the display is first turned on. The external supply voltages (VAN, VDD, and VPG) can all be applied at the same time as in the diagram. An internal power-on-reset signal is triggered when both the VAN and VDD voltages exceed a built-in threshold level. After a delay of about 70ms the internal dc-dc controller is activated which generates a negative supply for the common cathode of the array. The video display is enabled 20ms later and video is displayed on the array after the DISPOFF bit has been set to "0" via the serial port. Prior to this moment the pixels in the array are actively driven to the black state. The pin RESETB must also be logic high before any registers can be written.

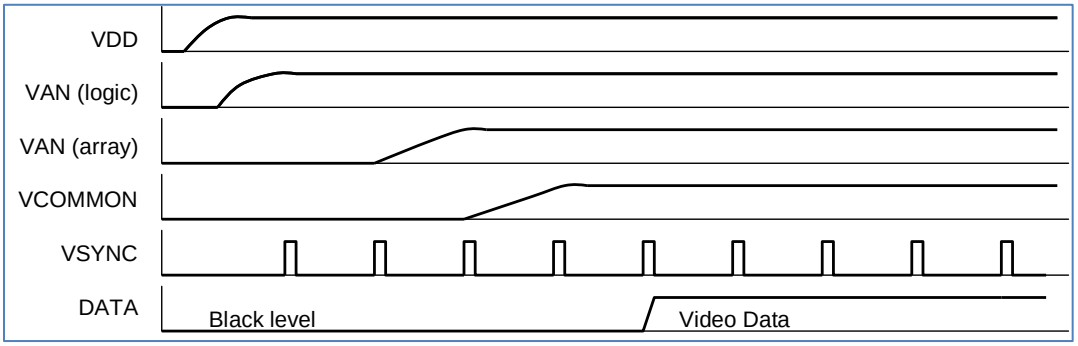


Figure 16 : Power-Up sequence for supplies and control.

During the power down operation, the supply rails should be switched off in the reverse order to the power up sequence. When the POR function detects a drop in the VDD supply below a minimum operating threshold it will immediately switch off the Row and Column sequencing circuits. At the same time the VCOMMON supply will be turned off followed by the 5V array supply. The power-down sequence is illustrated in Figure 17.

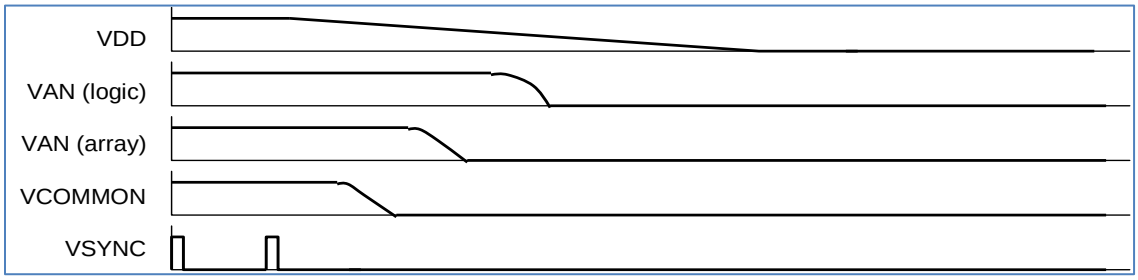


Figure 17: Power-Down sequence for supplies and control.

10.8.1 Software Reset Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the black state.. The DISPOFF bit (bit 5) in the DISPMODE register (Register 02) must be set to zero via the serial port in order for the array to become active.

10.9 Power Savings Modes

The circuit shall provide power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register SYSPWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control - many functional blocks have the option to be turned off individually via control of registers ANGPWRDN and SYSPWRDN.

10.10 Built-In Test Patterns

The IC includes functionality to simplify the external hardware requirements for test of OLED microdisplays and applications. The display is self-powered for this mode with no external video, sync, or clock signals required. The display starts in this mode with a simple, flat white field at maximum luminance by default and without the need for register setting.

The BI mode is activated at start-up when a dedicated pin Burn_In is set to logic level 1 or PATTEN bit in register TPMODE is set high. The internal dc-dc converter oscillator is used to generate the basic timing sequence (VSYNC, HSYNC, and SCLK). The vertical frequency will be set to 60Hz.

By default an all-pixels-on pattern will be displayed. The following extra test patterns are included and are accessed via the serial interface:

- 16 level gray scale, checkerboard, alternating rows and columns, cross-hatch line pattern
- Use bits PATTSEL in register TPMODE to select various patterns
- Use registers TPLINWTH, TPCOLSP, TPROWSP and TPCOLOR to customize the patterns

Figure 18 illustrates the application setup for the chip in BI mode using the built-in test functionality.

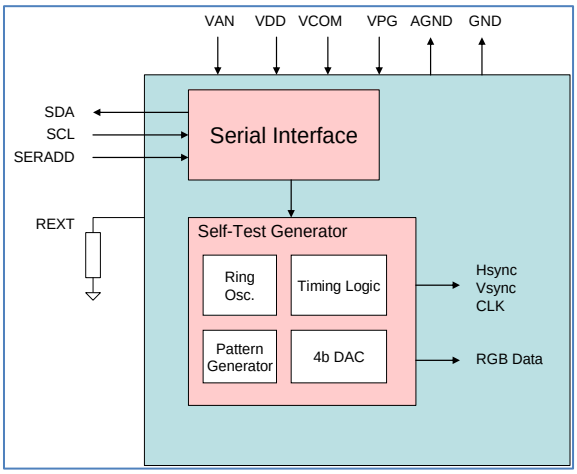


Figure 18 : Block diagram of setup for BI mode

11. REGISTER MAP SUMMARY

I2C Slave Address : 0100 11x

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STAT	R	REV	2-0	0	Silicon Revision Number
01	VINMODE	R/W	WRDISABLE	4	0	I^2C Register Write Disable 0 = Write Enable, 1 = Write Protected (Read Only)
			SET_ENABLE	3	0	ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high
			SET_FIELD	2	0	FIELD Polarity 0 = Odd Field when ENABLE=Active, 1 = Even Field when ENABLE=Active
			VSYNCPOL	1	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			HSYNCPOL	0	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
02	DISPMODE	R/W	DISPOFF	5	1	Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off
			3D-MODE	4	0	3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode
			SCMODE	3-2	0	Progressive or Interlaced scan mode select 00 = Progressive, 01 = Interlaced, 1X = Pseudo Interaced
			VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
			HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
03	LFTPOS	R/W		7-0	0C	Column Display Left Position
04	RGTPOS	R/W		7-0	0C	Column Display Right Position
05	TOPPOS	R/W		7-0	0C	Row Display Top Position
06	BOTPOS	R/W		7-0	0C	Row Display Bottom Position
07	ROWRESET	R/W		7-0	0	Row Duty Control
08				9-8		0:Disable, Each line displayed ROWRESET*2 Line period
09	RAMPCTL	R/W	Reserved	4	0	Do Not Change
			RAMPHIGH	3	0	Internal Ramp DAC set All High 0 = Normal operation, 1 = DAC set All High
			FLYBTIME	2	0	Ramp Fly back Time 0 = 800 nSec, 1 = 500 nSec
			RAMPDLY	1-0	1	Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK
0A	RAMPBOOST			1	0	Double current on Ramp Buffer current control
				0	0	Double current on Ramp Amp current control
0B	RAMPCM	R/W	RAMPMON	7	0	Internal Ramp Buffer Monitor Enable
			RAMPBCM	6-4	4	Ramp Buffer Current Control (000 = -75%(Don't use), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
			DACMON	3	0	Internal Ramp DAC Monitor Enable
			RAMPACM	2-0	4	Ramp Amp Current Control (000 = -75%(Don't use), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
0C	VDACMX	R/W		7-0	80	Ramp DAC Max Value Control, -40% ~ +40 %
0D	BIASN	R/W	EXT_VREF	3	0	External VREF Enable
			BIASN	2-0	1	000 = bias current off 001~101 = bias current set to 0.5nA, 1nA, 1.5nA, 2nA, 2.5nA 110~111 = Do Not Use (same as 2.5nA)
0E	GAMMASET	R/W	PMPCTRL	5-4	0	VCOM PUMP control when VGN sampling time 00=always enable, 01=hold when sampling, 10=only enable when VSYNC, 11=only enable when Fly back
			VGNSH_EN	3	0	VGN Sample & Hold Enable 0 = VGN SH Bypass, 1 = Enable VGN SH output
			IDSTEP	2-0	0	Current level for gamma sensor
0F	VCOMMODE	R/W	ISEN_EN	3-2	0	VCOM I-Sensor Enable
			VCOMAUTO	1-0	0	00 = AUTO1 mode 01 = Reserved - Do Not Use 10 = MANUAL mode
10	VCOMCTL	R/W	SS_BYPASS	7	0	VCOM Soft Start Bypass mode 0 = Soft Start function enable, 1 = Soft Start Bypass
			VCKDUTY	6-4	3	VCOM Clock Duty Control (High:Low) 0=1:7, 1=1:3, 2=3:5, 3=1:1, 4=5:3, 5=3:1, 6=7:1, 7=Don't use
			VCKSEL	3-2	3	VCOM Clock Select 0=125KHz, 1=250KHz, 2=500KHz, 3=800KHz
			VCOMSS	1-0	1	VCOM Soft Start Delay Time Mode 0 = 2mS, 1 = 4mS, 2 = 8mS, 3 = 16mS
11	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
12	VCOM	R/W		7-0	51	VCOM manual setting (used when VCOMMODE = 01 or 10 , default = -2.3V)
13	IDRF	R/W	IDRF_COARSE	7-5	1	Coarse adjustment for array reference current
			IDRF_FINE	4-0	10	Fine adjustment for array reference current

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
14	DIMCTL	R/W		6-0	64	Dimming level control (default = 1X IDRF)
15	TREFDIV	R/W		5-0	20	Temp. Sensor Reference Clock Divider
16	TEMPOFF	R/W		7-0	75	Temp. Sensor Offset
17	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * $PERIOD_{FRAME}$ $PERIOD_{FRAME}$ = 16.6 mSec when using 60Hz Video
18	TEMPOUT	RO		7-0	-	Temperature Sensor Readout
19	ANGPWRDN	R/W	ISENPD	7	0	ISEN Power Down
			IDMAXPD	6	0	IDMAX Power Down
			VCOMPD	5	0	VCOM Power Down
			VREFPD	4	0	VREF Power Down
			GMSENPD	3	0	Gamma Sensor Power Down
			VCSENPD	2	0	VCOM Sensor Power Down
			TSENPD	1	0	Temperature Sensor Power Down
			TREFPD	0	0	Temperature Reference Power Down
1A	SYSPWRDN	R/W	PDWN	5	0	All System Power Down (Override all analog power down, except POR50VPD, POR25VPD)
			LVDSPD	5	0	LVDS receiver Power Down
			RBUFPD	4	0	RAMP Buffer Power Down
			RAMPPD	3	0	RAMP DAC AMP Power Down
			DACPD	2	0	RAMP DAC Power Down
			POR50VPD	1	0	5V POR Power Down
			POR25VPD	0	0	2.5V POR Power Down
1B	TPMODE	R/W	TPVCLK	4	0	Enable external clock for Burn-in test mode (0=use internal ring OSC, 1=use external LVDS clock)
			PATTEN	3	0	Test Pattern Display Enable when "1"
			PATTSEL	2-0	0	Select test pattern for Built-In-Test-Mode (BURNIN pin = 'High' or PATTEN = 1) 000= Burn-in (all white), 001=Color Bar, 010=16 level gray scale 011=Checker Board, 100=Vertical Line, 101= Horizontal Line, 110=Grid Pattern
1C	TPLINWTH	R/W		7-0	0	Line Test Pattern Line Width (0=1pixel, 1=2pixel, ..., 255=256pixel)
1D	TPCOLSP	R/W		7-0	0	Line Test Pattern Column Space (0=1pixel, 1=2pixel, ..., 255=256pixel)
1E	TPROWSP	R/W		7-0	0	Line Test Pattern Row Spce (0=1pixel, 1=2pixel, ..., 255=256pixel)
1F	TPCOLOR	R/W	TPBGCLR	6-4	0	Line Test Pattern Background Color (RGB)
			TPFGCLR	2-0	7	Line Test Pattern Forground Color (RGB)
20	DLYSEL	R/W	SKWDLY	7-4	0	Select LVDS Skew Align reference Clock delay 0 = no delay, 1 = one unit delay, ... ,15 = 15 unit delay
			CLKDLY	3-0	6	Select clock delay for serial data latch 0 = no delay, 1 = one unit delay, ... ,15 = 15 unit delay
21	LVDSCTL	R/W	ALNMOD	2	0	LVDS Align mode 0 = normal Operation, 1 = auto align mode
			SKEWMOD	1-0	0	LVDS Skew mode 0 = normal Operation, 1 = auto skew, 2 = manual skew one set for all (use SKEW0), 3 = manual skew separate setting
22	SKEW0	R/W		7-0	0	LVDS data line #0 skew setting (when SKEWMOD=2, SKEW0 override others)
23				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
24	SKEW1	R/W		7-0	0	LVDS data line #1 skew setting
25				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
26	SKEW2	R/W		7-0	0	LVDS data line #2 skew setting
27				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
28	SKEW3	R/W		7-0	0	LVDS data line #3 skew setting
29				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
2A	SKEW4	R/W		7-0	0	LVDS data line #4 skew setting
2B				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
2C	SKEW5	R/W		7-0	0	LVDS data line #5 skew setting
2D				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
2E	SKEW6	R/W		7-0	0	LVDS data line #6 skew setting
2F				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
30	SKFAST	R	SKFAST	6-0	-	All "0" = OK, Not all "0" = Error (need decrease SKWDLY)
31	SKSLOW	R	SKSLOW	6-0	-	All "1" = OK, Not all "1" = Error (need increase SKWDLY)
32	SYNCMOD	R/W	DEFEN	2-1	1	define ENABLE/VS pin function 00=not used (all embeded), 01=used as ENABLE, 10=used as VSYNC
			DEFHS	0	0	define HS/ALIGN pin function 0 = use as ALIGN function only, 1 = used as HSYNC and ALIGN function
33	LUT_ADDR	R/W		7-0	0	Gamma Look-Up Table template access Address
34	LUT_DATA	R/W	LUT_DATAL	7-0	0	Gamma Look-Up Table template R/W Data LSB (Auto LUT_ADDR increase)
35			LUT_DATAH	9-8	0	Gamma Look-Up Table template R/W Data MSB
36	LUT_UPDATE	R/W	UDGAMMA	3	0	Update LUT template ro R,G,B Gamma LUT enable (Auto cleared after update)
			UDRGB	2-0	7	Select R,G,B Gamma LUT to update (ex. 100=R Gamma Update)
37	Reserved	R/W		3-0	0	Do Not Change
38	Reserved	R/W		4-0	0	Do Not Change
39	Reserved	R/W		7-0	0	Do Not Change

DETAILED REGISTER DESCRIPTIONS

11.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
REV	2-0	6	Silicon revision number; Rev. 1 = 0

Bits REV in this register indicate the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

11.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
WRDISABLE	4	0	I^2C register write disable
SET_ENABLE	3	0	ENABLE active level
SET_FIELD	2	0	Field polarity
VSYNCPOL	1	1	VSYNC polarity
HYSYNCPOL	0	1	HSYNC polarity

WRDISABLE:

1 = write protected (all other registers become read only)
0 = write enable (all registers can be updated externally via I^2C) (default)

SET_ENABLE:

0 = the active state of the ENABLE input is set “low” (default)
1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is

programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

The ENABLE input pin is also used to indicate field polarity in non-3D interlaced modes. In this mode the SET_FIELD bit determines the field polarity when ENABLE is active.

SET_FIELD:

0 = Odd Field when ENABLE=Active (default)
1 = Even Field when ENABLE=Active

The SET_FIELD register determines the field polarity of the video signal when the ENABLE pin is active.

VSYNCPOL:

0 = Negative Sync (default)
1 = Positive Sync

HSYNCPOL:

0 = Negative Sync (default)
1 = Positive Sync

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

11.3 DISPMODE (02h)

Name	DISPMODE
Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPOFF	5	1	Display On/Off control
3D-MODE	4	0	3D Mode control
SCMODE	3-2	0	Progressive or Interlaced scan mode selection
VSCAN	1	0	Vertical Scan direction
HSCAN	0	0	Horizontal Scan direction

DISPOFF:

0 = Display is turned ON
1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

3D-MODE:

0 = Normal display mode (default)
1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h). The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0", bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE="1", bit #3 of the VINMODE register). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

SCMODE:

00 = Progressive scan mode (default)
01 = Interlaced scan mode
1X = Pseudo-interlaced mode

Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field.

VSCAN:

0 = Top to Bottom vertical scan direction (default)
1 = Bottom to Top vertical scan direction

HSCAN:

0 = Left to Right horizontal scan direction (default)
1 = Right to Left horizontal scan direction

11.4 LFTPOS (03h)

Name	LFTPOS

Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Left position of first active column

This register, along with register RGTPOS, is used to set the horizontal position of the active display window within the 1944 available columns of pixels. In WUXGA mode the active window can be moved by +/-12 pixels from the center (default) position. When LFTPOS is increased, register RGTPOS must be decreased by the same value so that the sum of the two remains equal.

11.5 RGTPOS (04h)

Name	RGTPOS
Address	04h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Right position of last active column

This register, along with register LFTPOS, is used to set the horizontal position of the active display window within the 1944 available columns of pixels. In WUXGA mode the active window can be moved by +/-12 pixels from the center (default) position. When RGTPOS is increased, register LFTPOS must be decreased by the same value so that the sum of the two remains equal.

11.6 TOPPOS (05h)

Name	TOPPOS
Address	05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Top position of first active row

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 1224 available rows of pixels. In VGA mode the active window can be moved by +/-12 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

11.7 BOTPOS (06h)

Name	BOTPOS
Address	06h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Bottom position of last active row

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 1224 available rows of pixels. In VGA mode the active window can be moved by +/- 12 pixels from the center (default) position. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal.

11.8 ROWRESET (07h, 08h)

Name	ROWRESET
Address	07h, 08h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ROWRESETL (07h)	7-0	0	Row duty rate control (LSB)
ROWRESETH (08h)	9-8	0	Row duty rate control (MSB)

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

ROWRESET (dec)	Active Line Cycles	Active Duty Rate (%)	Note
0	all	100	Pixels active for entire frame period
1	2	$2*T_{HSYNC}/T_{FRAME}$	1249 total HS cycles / frame (WUXGA/85Hz)
n	2*n	$2*n*T_{HSYNC}/T_{FRAME}$	
>624	all	100	Pixels active for entire frame period

11.9 RAMPCTL (09h)

Name	RAMPCTL
Address	09h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	4	0	Reserved (Do Not Change)
RAMPHIGH	3	0	Set internal RAMP DAC high

FLYBTIME	2	0	RAMP Flyback time
RAMPDLY	1-0	1	RAMP delay in DCLK cycles

RAMPHIGH:

0 = Normal operation (default)
1 = DAC set to all high output

The RAMPHIGH register is used to set internal RAMPDAC to all high output mode for test purposes.

FLYBTIME:

0 = 500 ns (default)
1 = 800 ns

The FLYBTIME register is used to set the fly-back time for the internal RAMP.

RAMPDLY:

00 = - ½ DLCK
01 = no delay (default)
10 = + ½ DCLK

The RAMPDLY2 register is used to adjust the starting position of the internal RAMP.

11.10 Reserved (0Ah)

Name	Reserved
Address	0Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved (Do Not Change)

11.11 RAMPCM (0Bh)

Name	RAMPCM
Address	0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RAMPMON	7	0	Internal RAMP Amp monitor enable
RAMPBCM	6-5	4	RAMP Buffer current control
DACMON	3	0	Internal RAMP DAC monitor enable
RAMPACM	2-0	4	RAMP Amp current control

RAMPMON:

0 = Disable internal RAMP Buffer monitoring (default)
1 = Enable internal RAMP Buffer monitoring

The RAMPMON register is used to enable monitoring of the internal RAMP buffer output signal.

RAMPBCM:

000 = -75% (Do Not Use)
001 = -75%
010 = -50%
011 = -25%
100 = nominal (default)
101 = +25%
110 = +50%
111 = +75%

The RAMPBCM register is used to set the operating bias current for the internal RAMP buffer. The settings reduce or increase the current by a percentage of the nominal (default) value.

DACMON:

0 = Disable internal RAMP DAC monitoring (default)
1 = Enable internal RAMP DAC monitoring

The DACMON register is used to enable testing of the internal RAMP DAC output signal.

RAMPACM:

000 = -75% (Do Not Use)
001 = -75%
010 = -50%
011 = -25%
100 = nominal (default)
101 = +25%
110 = +50%
111 = +75%

The RAMPACM register is used to set the operating bias current for the internal RAMP amplifier. The settings reduce or increase the current by a percentage of the nominal (default) value.

11.12 VDACMX (0Ch)

Name	VDACMX
Address	0Ch

Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	RAMP DAC maximum value control

Register VDACMX is used to adjust the maximum value of the internal RAMP DAC signal by -40% to +40% of the nominal value.

NOTE: The normal operating value for VDACMX should be set to 78h.

The typical dependence of display luminance on VDACMX(dec) is shown in Figure 8. The luminance is seen to saturate for VDACMX greater than 79h in this sample. For normal operation VDACMX should be set to about 90 to 95% of the saturation value as shown in the figure.

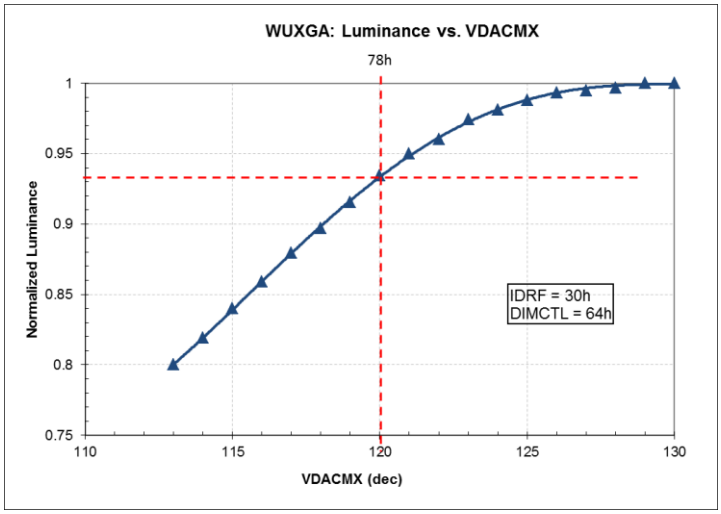


Figure 19: Luminance dependency on VDACMX

11.13 BIASN (0Dh)

Name	BIASN
Address	0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
EXT_VREF	3	0	Enable external VREF
BIASN	2-0	1	Set pixel bias current

EXT_VREF:

1 = enable the external VREF source
0 = use the internal VREF source (default)

Note: This option not available on the current package – use the default setting only.

BIASN:

000 = pixel bias current is turned off
001 = pixel bias current set to 0.5nA (default)
010 = pixel bias current set to 1.0 nA
011 = pixel bias current set to 1.5 nA
100 = pixel bias current set to 2 nA
101 = pixel bias current set to 2.5 nA
110 ~111 = Do not use

The BIASN register is used to set the sink current applied in each pixel cell. It is recommended to use the BIASN=03 setting in normal operation.

11.14 GAMMASET (0Eh)

Name	GAMMASET
Address	0Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PMPCTRL	5-4	0	VCOM pump hold enable during VGN sampling
VGNSH_EN	3	0	VGN sample & hold enable
IDSTEP	2-0	0	Current level for gamma sensor

PMPCTRL:

00 = Normal operation, pump hold disabled (default)
01 = Enable pump hold during VGN sampling time
10 = Enable only VSYNC period
11 = Enable only Flyback period

The PMPCTRL register is used to disable the VCOM converter switch during the VGN sampling time to reduce noise pickup.

VGNSH_EN:

0 = Bypass the VGN sample & hold function (default)
1 = Enable the VGN sample & hold function

The VGNSH_EN register is used to activate the internal sample & hold function provided at the VGN output pin.

IDSTEP:

0h ≈ IDRF/128
1h ≈ IDRF/64
2h ≈ IDRF/32
3h ≈ IDRF/16
4h ≈ IDRF/8
5h ≈ IDRF/4
6h ≈ IDRF/2
7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

11.15 VCOMMODE (0Fh)

Name	VCOMMODE
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISEN_EN	3-2	0	Enable the VCOM current sensor
VCOMAUTO	1-0	0	Set internal VCOM supply mode

ISEN_EN:

TBD

VCOMAUTO:

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
01 = AUTO2 mode
10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.
In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.
In the Auto 3 mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

11.16 VCOMCTL (10h)

Name	VCOMCTL
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SS_BYPASS	7	0	Bypass the VCOM soft start mode
VCKDUTY	6-4	3	VCOM clock duty control
VCKSEL	3-2	3	VCOM clock select
VCOMSS	1-0	1	VCOM soft start delay time

SS_BYPASS:

0 = Normal operation, soft-start function enabled (default)
1 = Disable the VCOM soft-start function

VCKDUTY:

0h = 1:7
1h = 1:3
2h = 3:5
3h = 1:1 (default)
4h = 5:3
5h = 3:1
6h = 7:1
7h = don’t use

Register VCKDUTY sets the VCOM clock duty ratio (high:low).

VCKSEL:

0h = Generate Custome VCOM clock with NVCK0/NVCK1 Reg.
(See NVCK0/NVCK1 description
1h = 250 kHz
2h = 500 kHz
3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.

VCOMSS:

0h = 2 ms
1h = 4 ms (default)
2h = 8 ms

3h = 16 ms

Register VCMOSS sets the soft-start duration during startup of the VCOM converter.

11.17 VGMAX (11h)

Name	VGMAX
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

00h = 5 (VAN = 5V)
0Dh = 4.95 (default)
FFh = 4

VGMAX level = VAN*(1 - 0.2*VGMAX(dec) / 255)

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VAN supply to prevent saturation of the video buffer amplifiers.

11.18 VCOM (12h)

Name	VCOM
Address	12h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	**51***	40	30
Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	**-2.4**	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE =01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply ≈ -2.3V.

The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 20 for a color display.

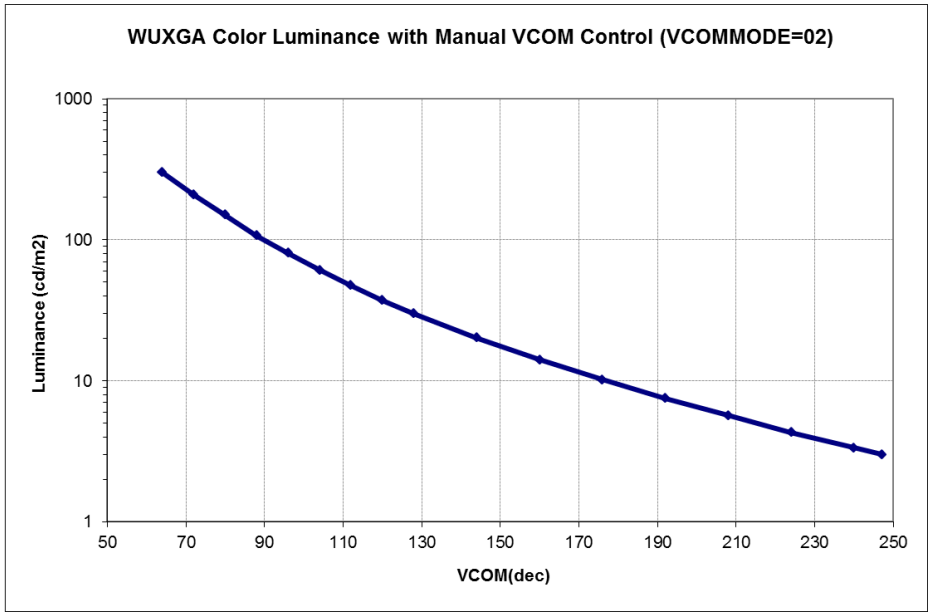


Figure 20: Typical luminance dependency on manual VCOM setting

11.19 IDRF (13h)

Name	IDRF
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
IDRF_FINE	4-0	01	Fine adjustment for array reference current

IDRF_COARSE:

IC#
0h = 0 (default)
1h = 0.5
2h = 1.5
3h = 2.5
4h = 3.5

IDRF_FINE:

IF#

00h = 0
01h = 1/32 (default)
…
10h = 16/32
…
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF given by the following expression:

$LMAX = LDEF*(IC\# + IF\#)$ in cd/m^2

where the luminance for a color display is LDEF ≈ $100cd/m^2$ at the default settings (see table below).

IDRF (hex)	LMAX / LDEF
0	0
10	0.5
20	0.5
30	1
40	1.5
50	2
60	2.5
70	3
80	3.5

11.20 DIMCTL (14h)

Name	DIMCTL
Address	14h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	01	Dimming level control

00h = 0
01h = 1% of LMAX
…
64h = 100% of LMAX
…
7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 01h is equal to 1% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

11.21 TREFDIV (15h)

Name	TREFDIV
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	28	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.22 TEMPOFF (16h)

Name	TEMPOFF
Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	D7	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.23 TUPDATE (17h)

Name	TUPDATE
Address	17h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

Update Time = (TUPDATE(decimal) + 1)*T_{FRAME}

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

11.24 TEMPOUT (18h)

Name	TEMPOUT
Address	18h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The VGA display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (17H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX}, the expected sensor response would be as follows:

$$TEMPOUT\,(dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$

$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60ºC to +80ºC are given by the following values for package A04-500463-01:

$$TREFDIV(d) = 25$$
$$TEMPOFF(d) = 93$$

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum value for TEMPOFF which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=25d=19h and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0ºC, 20ºC, 40ºC, 60ºC
- Take the slope to find the sensor response, A_{MEAS} = dTEMPOUT(d)/dtemp
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=25d=19h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read $TEMPOUT_{AMB}$ and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - TEMPOUT_{AMB}$$

With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(°C) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60ºC will return a TEMPOUT reading of 0 and temperatures above +80ºC will return a hexadecimal value of FF.

11.25 ANGPWRDN (19h)

Name	ANGPWRDN
Address	19h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISENPD	7	0	ISEN power down
IDMAXPD	6	0	IDMAX power down
VCOMPD	5	0	VCOM power down
VREFPD	4	0	VREF power down
GMSENPD	3	0	Gamma sensor power down
VCSENPD	2	0	VCOM sensor power down
TSENPD	1	0	Temperature sensor power down
TREFPD	0	0	Temperature reference power down

ISENPD:

1 = VCOM current limit sensor is powered down
0 = normal operation (default)

IDMAXPD:

1 = IDMAX function is powered down
0 = normal operation (default)

VCOMPD:

1 = VCOM generator is powered down
0 = normal operation (default)

VREFPD:

1 = the VREF reference source is powered down
0 = normal operation (default)

GMSENPD:

1 = the Gamma sensor is powered down
0 = normal operation (default)

VCSNEPD:

1 = the VCOM sensor is powered down
0 = normal operation (default)

TSENPD:

1 = the Temperature Sensor is powered down
0 = the Temperature Sensor is operating normally (default)

TREFPD:

1 = the Temperature reference is powered down
0 = normal operation (default)

11.26 SYSPWRDN (1Ah)

Name	SYSPWRDN
Address	1Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PDWN	6	0	All systems power down
LVDSPD	5	0	LVDS receiver power down
	4	0	Reserved (Do Not Change)
RAMPPD	3	0	RAMP DAC amp and buffer power down
DACPD	2	0	RAMP DAC power down
POR50VPD	1	0	5V power-on-reset power down
POR25VPD	0	0	2.5V power-on-reset power down

PDWN:

1 = all systems are powered down
0 = normal operation (default)

By setting the PDWN bit to a "1" the chip enters a deep sleep mode in which all functions including the I^2C interface are powered down in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I^2C input lines and resets the PDWN bit when it detects the correct I^2C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

LVDSPD:
1 = LVDS receiver is powered down
0 = normal operation (default)

RAMPPD:

1 = internal RAMP DAC amplifier and buffer are powered down
0 = normal operation (default)

DACPD:

1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

POR50VPD:

1 = the 5V power-on-reset circuit is powered down
0 = normal operation (default)

POR25VPD:

1 = the 2.5V power-on-reset circuit is powered down
0 = normal operation (default)

11.27 TPMODE (1Bh)

Name	TPMODE
Address	1Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PATTEN	3	0	Enable test pattern display
PATTSEL	2-0	0	Select test pattern for Burn-In mode

The BI pin is tied high or PATTEN register set to high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)
001 = color bars
010 = gray scale (without gamma correction)
011 = checkerboard pattern
100 = alternating columns pattern
101 = alternating rows pattern
110 = grid pattern
111 = all black

Use with registers TPLINWTH, TPCOLSP, TPROWSP and TPCOLOR to modify the patterns according to the following table.

Test Pattern Name	TPMODE (17H)	TPLINWTH (18H)	TPCOLSP (19H)	TPROWSP (1AH)	TPFGCLR (1BH:2-0)	TPBGCLR (1BH:6-4)
All White	000	X	X	X	X	X
Color Bar	001	X	X	X	X	X
Gray Scale	010	X	X	X	X	X
Checker Board	011	X	X	X	X	X
Alternating Column	100	LW	CS	X	111	000
Alternating Row	101	LW	X	RS	111	000
Grid Pattern	110	LW	CS	RS	111	000
All Black	101	X	X	X	000	000
All White	101	X	X	X	111	111
All Red	101	X	X	X	100	100
All Green	101	X	X	X	010	010
All Blue	101	X	X	X	001	001

X: Don't care, LW: Line Width (0~255), CS: Column Space (0~255), RS: Row Space (0~255)

11.28 TPLINWTH (1Ch)

Name	TPLINWTH
Address	1Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern line width

This register is used to set the line width for the line-type test patterns.

0 = 1 pixel wide (default)
1 = 2 pixel wide
…
255 = 256 pixel wide

11.29 TPCOLSP (1Dh)

Name	TPCOLSP
Address	1Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern column spacing

This register is used to set the column spacing for the column-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

11.30 TPROWSP (1Eh)

Name	TPROWSP
Address	1Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern row spacing

This register is used to set the row spacing for the row-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

11.31 TPCOLOR (1Fh)

Name	TPCOLOR
Address	1Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TPBGCLR	6-4	0	Test pattern background color
TPFGCLR	2-0	7	Test pattern foreground color

This register is used to set the background and foreground colors (RGB) for certain test patterns.

11.32 DLYSEL (20h)

Name	DLYSEL
Address	20h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKWDLY	7-4	0	LVDS skew align reference clock delay
CLKDLY	3-0	6	LVDS clock delay for serial data latch

SKWDLY :
0 = Base delay
1 = Base delay + 1 unit delay
…
15 = Base delay + 15 unit delay
CLKDLY :
0 = Base delay
1 = Base delay + 1 unit delay
…
15 = Base delay + 15 unit delay

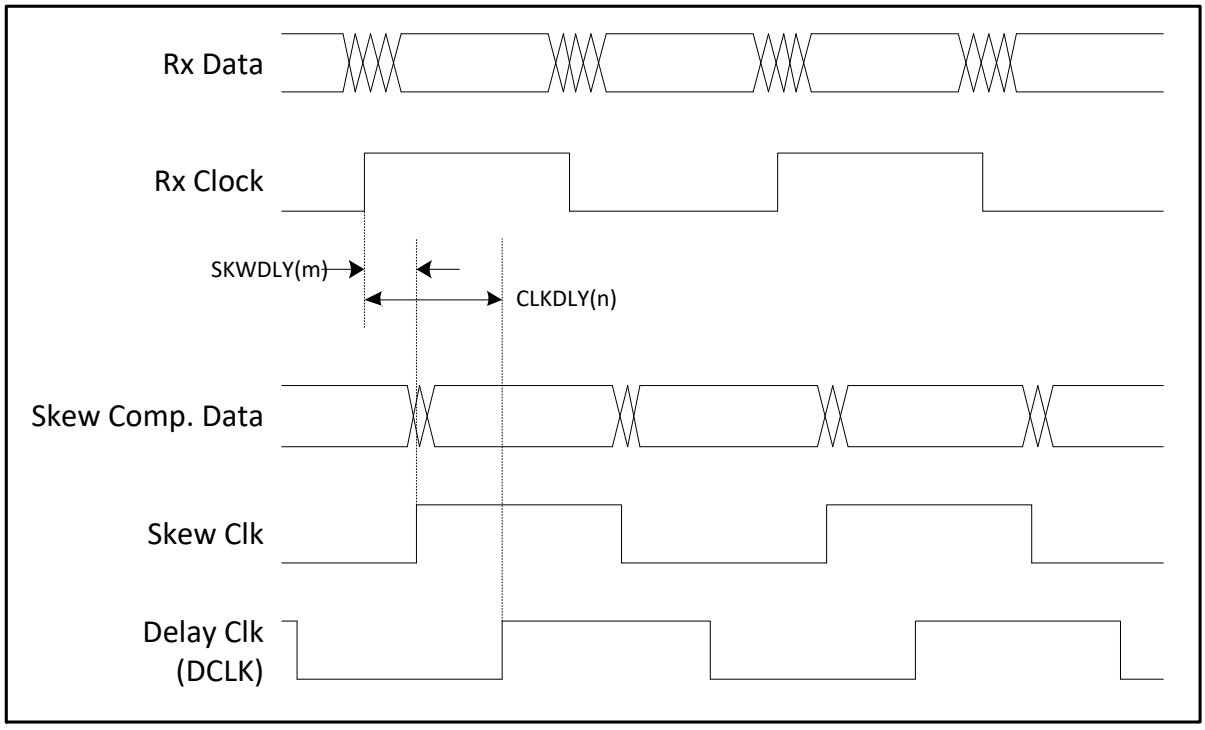


Figure 21: LVDS Skew compensation timing diagram

11.33 LVDSCTL (21h)

Name	LVDSCTL

Address	21h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ALNMOD	2	0	Enable LVDS align mode
SKEWMOD	1-0	0	Select skew compensation mode

ALNMOD :

1 = Enable LVDS align mode

- LVDS Tx should send proper align pattern (10000000) on LVDS_DAT2 with ALIGN signal
- Don't set with SKEWMOD = 1 (auto skew compensation mode)

0 = Disable LVDS align mode (stay current align setting and any ALIGN and align pattern input are ignored)

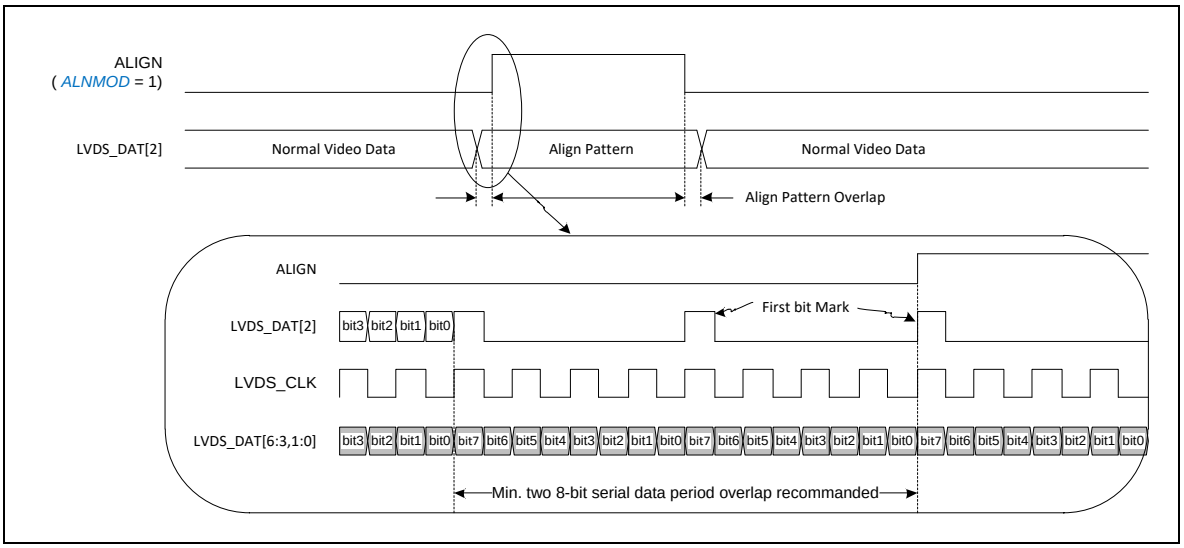


Figure 22: LVDS Align pattern

ALNMOD should set before activate ALIGN signal and reset after deactivate ALIGN signal.

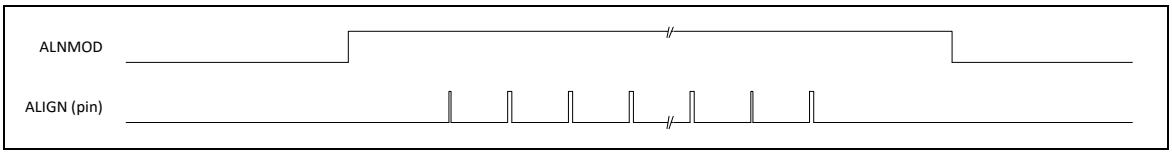


Figure 23: ALIGN signal example

SKEWMOD:

0 = Normal operation mode (stays current skew delay setting and no change)

1 = Automatic skew delay setting mode

- LVDS Tx should send proper Skew compensation pattern (00001111) on all data and clock

2 = Manual common skew delay setting mode (SKEW0 delay setting is used on all data line delay)
3 = Manual separate skew delay setting mode

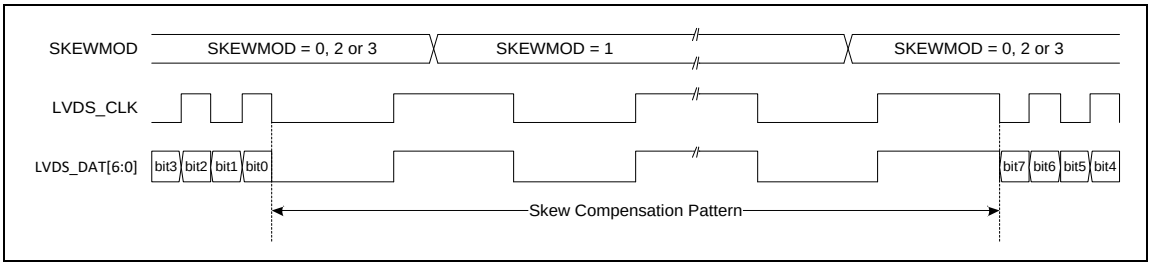


Figure 24: Skew compensation pattern

The SKEWMOD register operation is only valid while LVDS TX is sending the skew compensation pattern.

11.34 SKEW0 (22h, 23h)

Name	SKEW0
Address	22h, 23h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW0 (22h)	7-0	0	data line #0 delay setting lower byte
SKEW0 (23h)	15-8	0	data line #0 delay setting upper byte

00000000 00000000 = Base delay setting
00000000 00000001 = Base + 1 unit delay setting
00000000 00000011 = Base + 2 unit delay setting
00000000 00000111 = Base + 3 unit delay setting
00000000 00001111 = Base + 4 unit delay setting
:
01111111 11111111 = Base + 14 unit delay setting
11111111 11111111 = Base + 15 unit delay setting

I^2C register SKEW0~SKEW6 read out are always current working delay value

- SKEWMOD = 0 or 1 : current auto skew compensated values are read
- SKEWMOD = 2 : SKEW0 register value is applied to all other skew resister and read on all SKEW0~SKEW6
- SKEWMOD = 3 : each SKEWi register values are applied and read

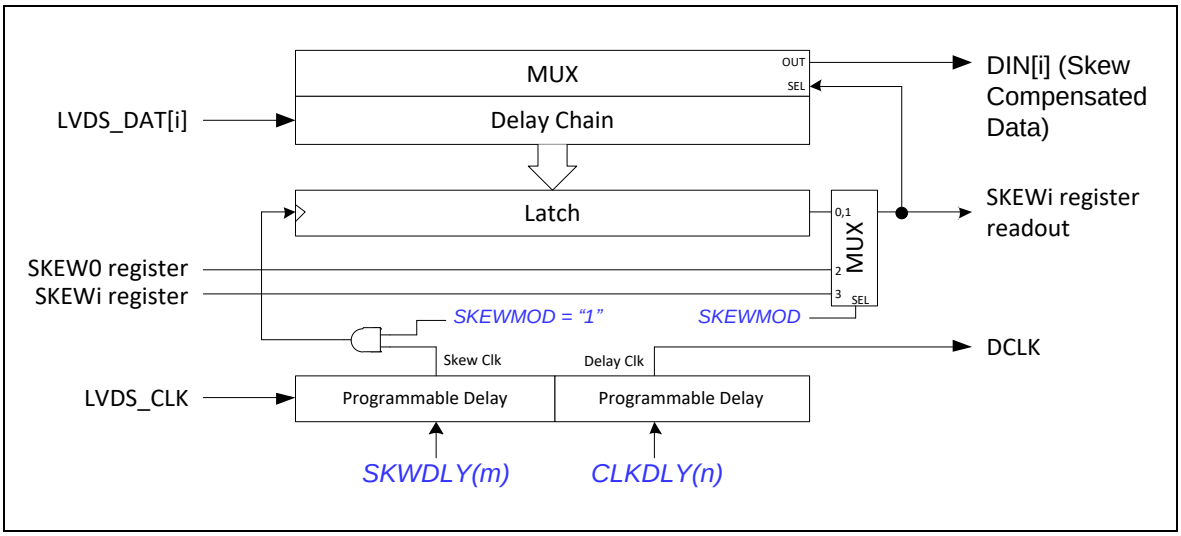


Figure 25: Skew compensation block diagram

11.35 SKEW1 (24h, 25h)

Name	SKEW1
Address	24h, 25h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW1 (24h)	7-0	0	data line #1 delay setting lower byte
SKEW1 (25h)	15-8	0	data line #1 delay setting upper byte

11.36 SKEW2 (26h, 27h)

Name	SKEW2
Address	26h, 27h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW2 (26h)	7-0	0	data line #2 delay setting lower byte
SKEW2 (27h)	15-8	0	data line #2 delay setting upper byte

11.37 SKEW3 (28h, 29h)

Name	SKEW3
Address	28h, 29h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description

SKEW3 (28h)	7-0	0	data line #3 delay setting lower byte
SKEW3 (29h)	15-8	0	data line #3 delay setting upper byte

11.38 SKEW4 (2Ah, 2Bh)

Name	SKEW4
Address	2Ah, 2Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW4 (2Ah)	7-0	0	data line #4 delay setting lower byte
SKEW4 (2Bh)	15-8	0	data line #4 delay setting upper byte

11.39 SKEW5 (2Ch, 2Dh)

Name	SKEW5
Address	2Ch, 2Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW5 (2Ch)	7-0	0	data line #5 delay setting lower byte
SKEW5 (2Dh)	15-8	0	data line #5 delay setting upper byte

11.40 SKEW6 (2Eh, 2Fh)

Name	SKEW6
Address	2Eh, 2Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW6 (2Eh)	7-0	0	data line #6 delay setting lower byte
SKEW6 (2Fh)	15-8	0	data line #6 delay setting upper byte

11.41 SKFAST (30h)

Name	SKFAST
Address	30h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
SKFAST	6-0	-	All “0’ after skew compensation => OK

Bit 15 of SKEW0 ~ SKEW6. If any of SKFAST bit is read as “1” after skew compensation then that line comes to much faster than selected skew clock. Decrease SKWDLY setting if possible.

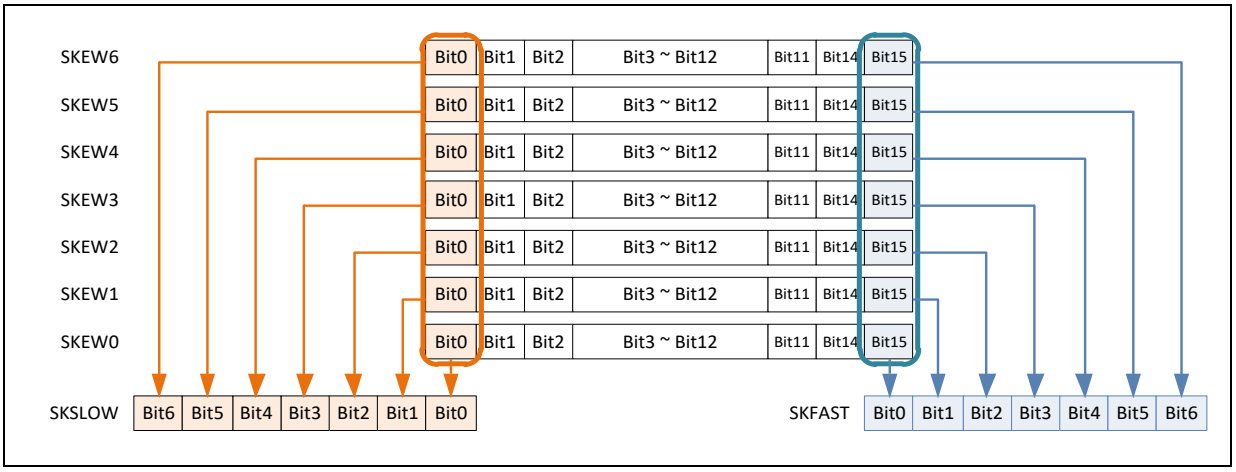


Figure 26: SKFAST and SKSLOW register mapping

11.42 SKSLOW (31h)

Name	SKSLOW
Address	31h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
SKSLOW	6-0	0	All “1” after skew compensation => OK

Bit 0 of SKEW0 ~ SKEW6. If any of SKSLOW bit is read as “0” after skew compensation then that line comes to much slower than selected skew clock. Increase SKWDLY setting if possible.

11.43 SYNCMOD (32h)

Name	SYNCMOD
Address	31h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DEFEN	2-1	1	Define ENABLE pin function
DEFHS	0	0	Define LVDS_ALGN pin function

DEFEN:

0 = Do not use ENABLE pin (ENABLE & VSYNC signal uses thru LVDS data lines)

1 = ENABLE pin used as ENABLE (Default)
2 = ENABLE pin used as VSYNC
3 = Do not use

DEFHS:
0 = LVDS_ALGN pin used as ALIGN function
1 = LVDS_ALGN pin used as ALIGN & HSYNC function

11.44 LUT_ADDR (33h)

Name	LUT_ADDR
Address	33h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_ADDR	7-0	0	Gamma look-up table template access address

11.45 LUT_DATA (34h, 35h)

Name	LUT_DATA
Address	34h, 35h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_DATAL (34h)	7-0	0	Gamma look-up table template R/W data LSB
LUT_DATAH (35h)	9-8	0	Gamma look-up table template R/W data MSB

When LUT_DATAL(34h) register is written following operations are happen
- Write Gamma look-up table template memory to LUT_DAT (10bit) data at current LUT_ADDR address. The MSB data should be written first.
- Increase LUT_ADDR register by 1 after write operation

When LUT_DATA register are read following data are read
- Current LUT_ADDR address data of Gamma look-up table memory are read

11.46 LUT_UPDATE (36h)

Name	LUT_UPDATE
Address	36h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
BPGAMMA	5	0	Gamma Bypass Enable

Reserved	4	0	Should be 0
UDGAMMA	3	0	Update LUT template to R,G,B LUT memory
UDRGB	2-0	7	Select R,G,B Gamma LUT for Update

BPGAMMA:
0 = Normal Operation with Gamma LUT Memory
1 = Gamma LUT Memory in video pass will be bypassed.

UDGAMMA
0 = No operations happen
1 = Enable copy LUT template memory data to selected R,G,B Gamma LUT memory

UDGAMMA register operation
- R,G,B LUT memory update is started at first VSYNC rising edge meet after UDGAMMA register set to 1
- UDGAMMA register cleared to 0 after update operation end automatically

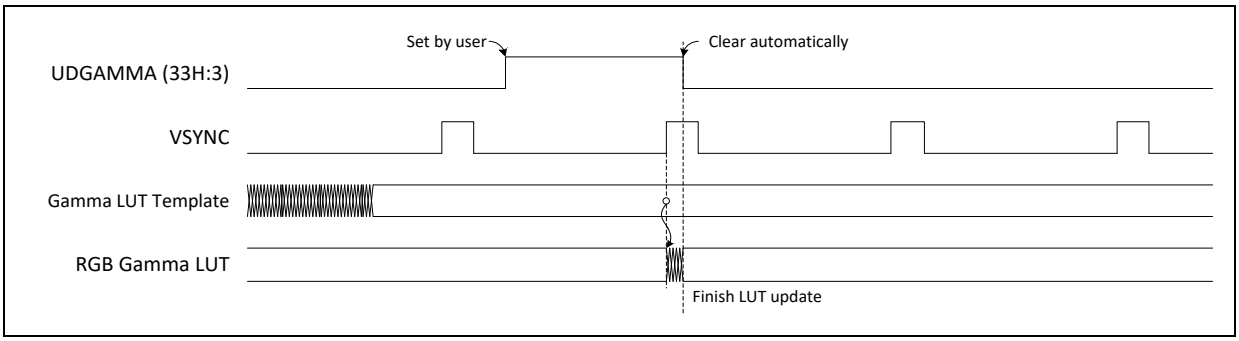


Figure 27: Gamma LUT Update timing

UDRGB:
001 = Select B Gamma LUT memory updated
010 = Select G Gamma LUT memory updated
011 = Select G, B Gamma LUT memory updated
100 = Select R Gamma LUT memory updated
101 = Select R, B Gamma LUT memory updated
110 = Select R, G Gamma LUT memory updated
111 = Select R, G, B Gamma LUT memory updated

11.47 Reserved (37h – 57h)

Name	Reserved
Address	37h -57h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	x	Reserved (Do Not Change)

11.48 NVCK0 (58h)

Name	NVCK0
Address	58h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	99	No. of VCLK for ”0” time of VcomClk when VCKSEL=0

NVCK0:

When VCKSEL =0, NVCK0 with NVCK1 are used to generate arbitrary VCOM clock frequency and duty based on the following equations.

VcomClk (Frequency) = f_{VCLK} * (1/((NVCK0+1) + (NVCK1 +1)))
VcomClk (Duty) = (NVCK1+1) / ((NVCK0+1)+(NVCK1+1))

*= f_{VCLK} is a half of the Pixel Clock of the 24 bit RGB source video

11.49 NVCK1 (59h)

Name	NVCK1
Address	59h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	99	No. of VCLK for ”1” time of VcomClk when VCKSEL=0

NVCK1:

See above NVCK0 descriptions.

12. TYPICAL REGISTER SETTINGS

I^{2}C slave address: 010011X

00h: STATUS	06	15h: TREFDV	26	2Ah: SKEW4L	7F	3Fh: HITMPH	00	54h: CF4	00
01h: VINMODE	03	16h: TMPFF	D7	2Bh: SKEW4H	00	40h: LUT0L	00	55h: CF5	00
02h: DISPMODE	00	17h: TUPDTE	FF	2Ch: SKEW5L	FF	41h: LUT0H	00	56h: CF6	00
03h: LFTPOS	0C	18h: TEMPOUT	98	2Dh: SKEW5H	00	42h: LUT1L	00	57h: CF7	00
04h: RGTPOS	0C	19h: ANGPRDN	00	2Eh: SKEW6L	7F	43h: LUT1H	00	58h: NVCK0	00
05h: TOPPOS	0C	1Ah: SYSPRDN	00	2Fh: SKEW6H	00	44h: LUT2L	00	59h: NVCK1	00
06h: BOTPOS	0C	1Bh: TPMODE	00	30h: SKFAST	00	45h: LUT2H	00	5Ah: NFPIXL	80
07h: ROWRSTL	00	1Ch: TPLNWTH	00	31h: SKSLOW	7F	46h: LUT3L	00	5Bh: NFPIXH	07
08h: ROWRSTH	00	1Dh: TPCOLSP	00	32h: SYNCMD	02	47h: LUT3H	00	5Ch: NFLNL	B0
09h: RAMPCTL	01	1Eh: TPROWSP	00	33h: LT_ADDR	FF	48h: LUT4L	00	5Dh: NFLNH	04
0Ah: RAMPBST	00	1Fh: TPCOLOR	07	34h: LT_DTL	FF	49h: LUT4H	00		
0Bh: RAMPCM	44	20h: DLYSEL	10	35h: LT_DTH	03	4Ah: LUT5L	00		
0Ch: VDACMX	80	21h: LVDSCTL	04	36h: LT_UPDT	07	4Bh: LUT5H	00		
0Dh: BIASN	03	22h: SKEW0L	FF	37h: PUCTRL	00	4Ch: LUT6L	00		
0Eh: GMMAT	07	23h: SKEW0H	00	38h: HIDDEN	00	4Dh: LUT6H	00		
0Fh: VCoMMDE	04	24h: SKEW1L	FF	39h: DIGTST	00	4Eh: LUT7L	00		
10h: VCOMCTL	3D	25h: SKEW1H	00	3Ah: RSV	00	4Fh: LUT7H	00		
11h: VGMAX	0D	26h: SKEW2L	7F	3Bh: SLOPE	00	50h: CF0	00		
12h: VCOM	51	27h: SKEW2H	00	3Ch: TCNTL	3E	51h: CF1	00		
13h: IDRF	48	28h: SKEW3L	FF	3Dh: TCNTH	02	52h: CF2	00		
14h: DIMCTL	64	29h: SKEW3H	00	3Eh: HITMPL	00	53h: CF3	00		

Figure 28: Screen snapshot of GUI showing typical register settings for WUXGA mode

Note: Register 00 (STATUS) shows the silicon version (06) and is a read-only register

13. APPENDIX A: APPLICATION SYSTEM DIAGRAM

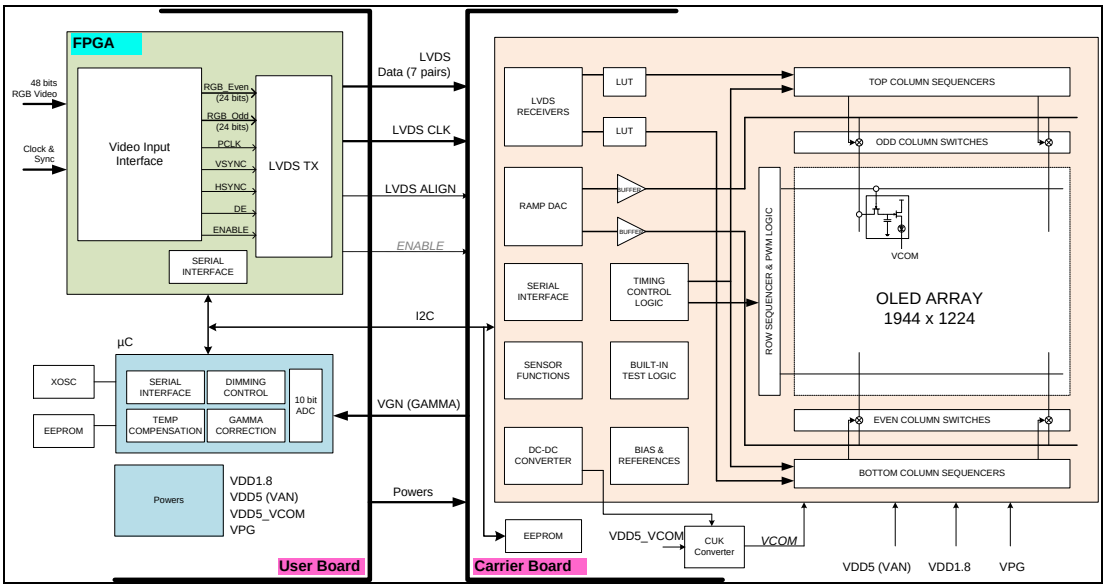
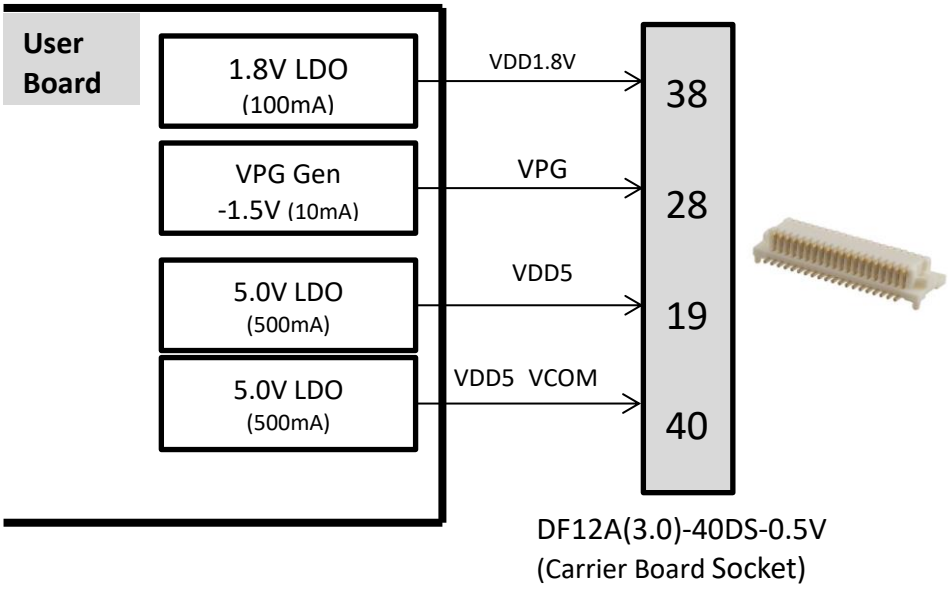


Figure A-1 : Block diagram of application reference system



The 5V LDO with higher current rating is better for VDD5. The power noise in VDD5 is sensitive to the Display noise.

Figure A-2 : Recommended Power Scheme for WUXGA-R5 Application

APPENDIX B: LVDS TRANSMITTER DESIGN EXAMPLE

The LVDS Transmitter block resides in the host system FPGA (or an independent FPGA, depending on the system design). This block encodes both data and control signals into a set of LVDS channels, according to the port mapping shown below in Table B-1. The transmitter uses a dedicated line pair for transmitting the clock signal, allowing the received to operate without a clock recovery circuit, which saves power.
The Verilog source code for this function is provided below. It is the same code as used in the eMagin Corporation Design Reference Kit FPGA.

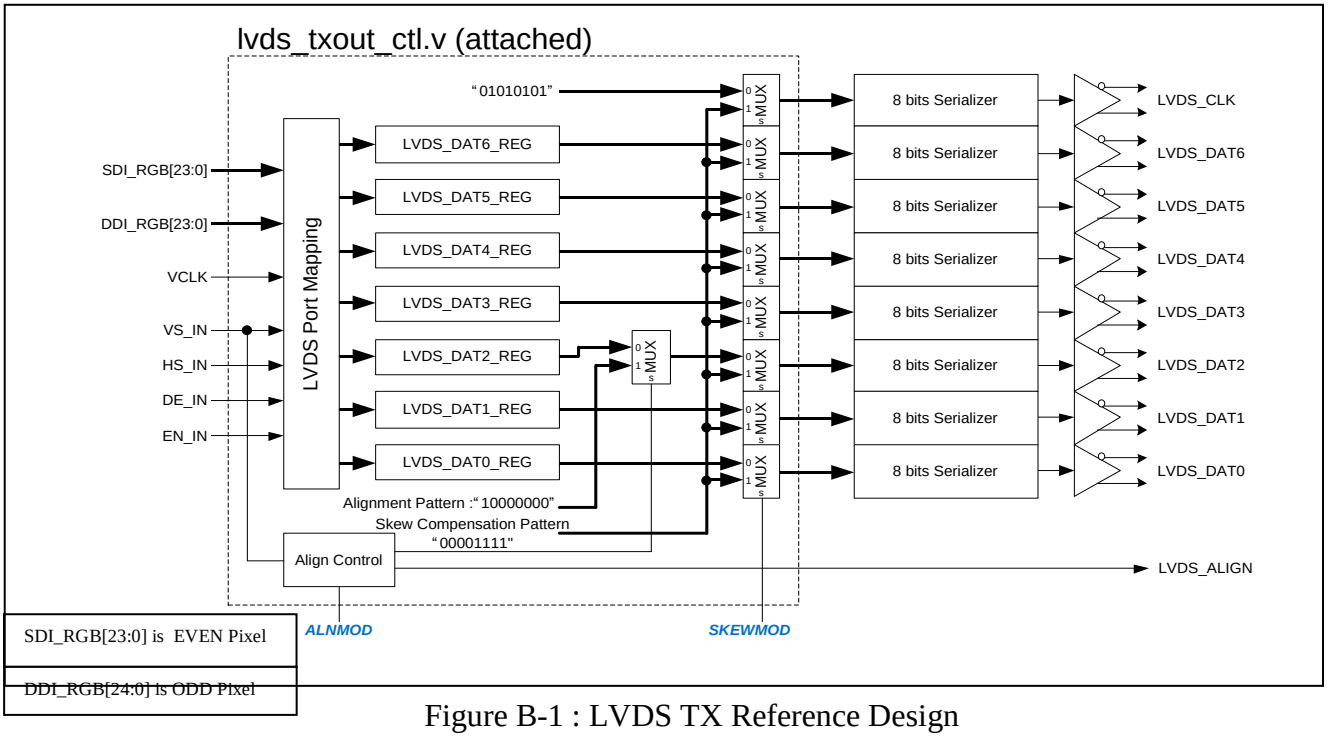


Figure B-1 : LVDS TX Reference Design

In addition to encoding the data and control lines, the LVDS Transmitter also includes a logic block aimed at providing for an automatic alignment between clock and data at the receiver side (the display), and at allowing for a compensation of the skew between data pairs.

Two control signals (ALNMOD and SKEWMOD) are needed for the alignment and skew compensation functions respectively. These two bits can be designed into a control register residing inside the FPGA and accessible via an i2c interface (this is how the functionality is implemented in the eMagin Corporation Design Reference Kit).

The LVDS TX (Transmitter) block, in addition of the lvds pairs, must also output the LVDS_ALGN signal (CMOS output level) to the display.

ALNMOD signal: When it is set, which is FPGA register, the LVDS Transmitter circuit should send the alignment pattern using the 3rd LVDS data channel and send the LVDS_ALIGN signal which is CMOS output. The alignment pattern is “10000000”. The LVDS_ALIGN signal and align pattern should be generated during inactive video period The Fig B-2 shows that it is generated during DE is inactive. We recommend generating it during VSYNC period.

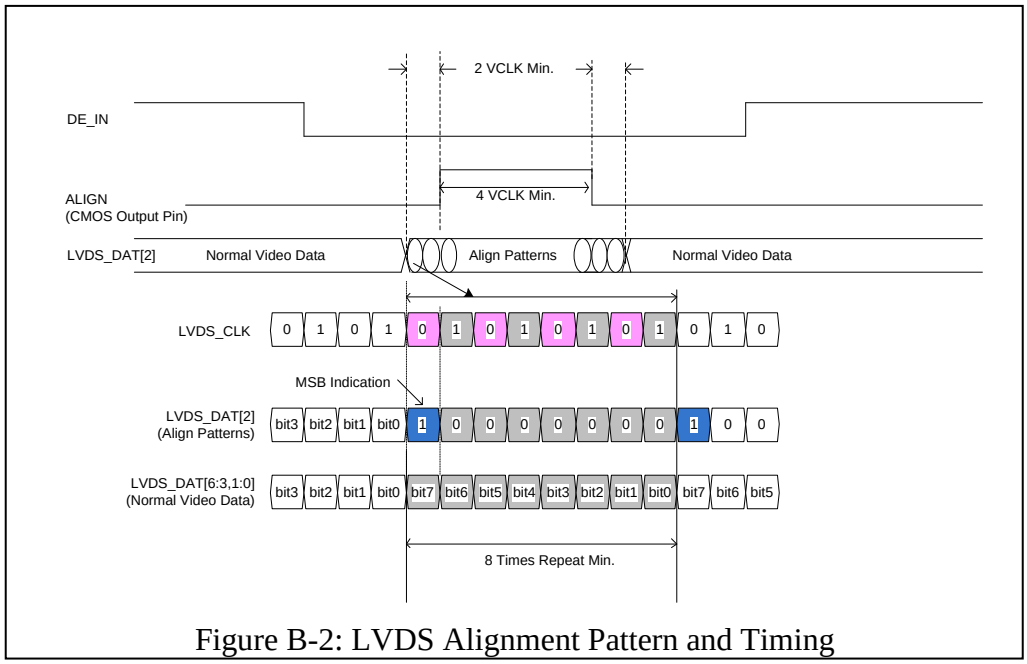


Figure B-2: LVDS Alignment Pattern and Timing

SKEWMOD signal: When it is set, which is FPGA reg, the TX should send the skew compensation patterns through all of the LVDS channel including the clock channel. The skew compensation pattern is “00001111”.

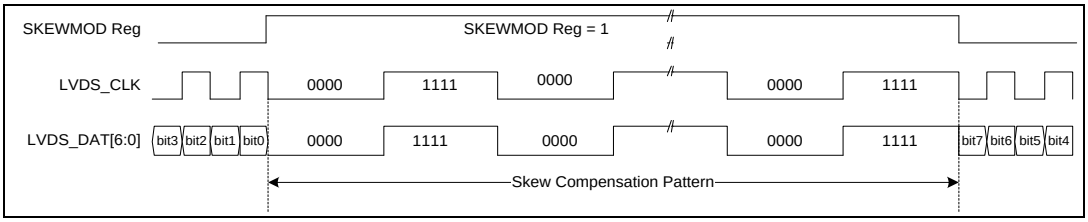


Figure B-3: LVDS Skew Compensation Pattern and Timing

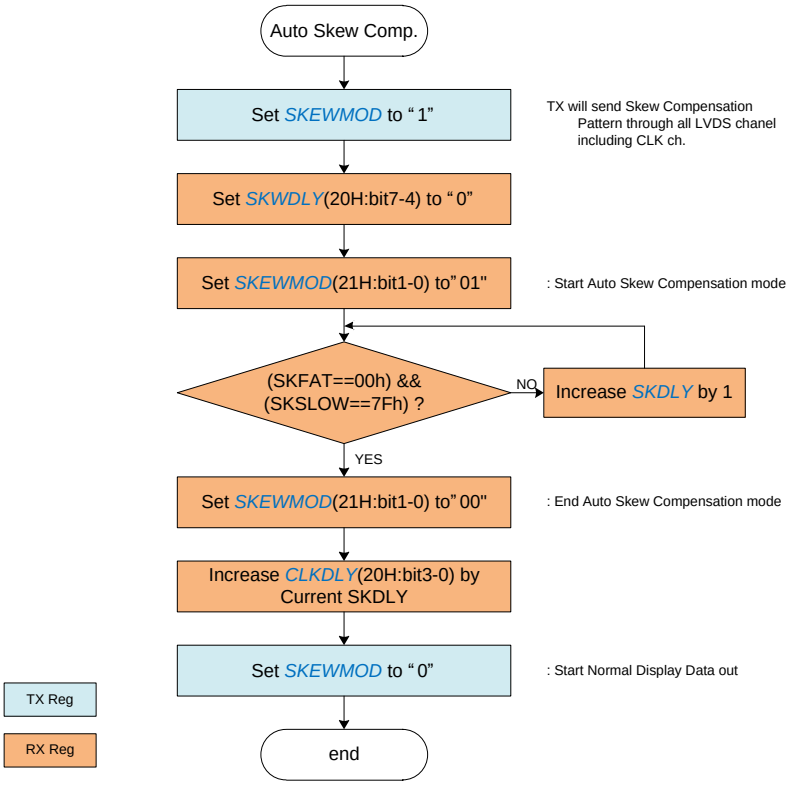
Alignment and Skew Compensation Operation

Skew Compensation

This function is typically performed at power on and its sequence is shown in the flow chart below:

Note that there are two SKEWMOD signals: one in the Transmitter (TX) block and one in the microdisplay (RX) .

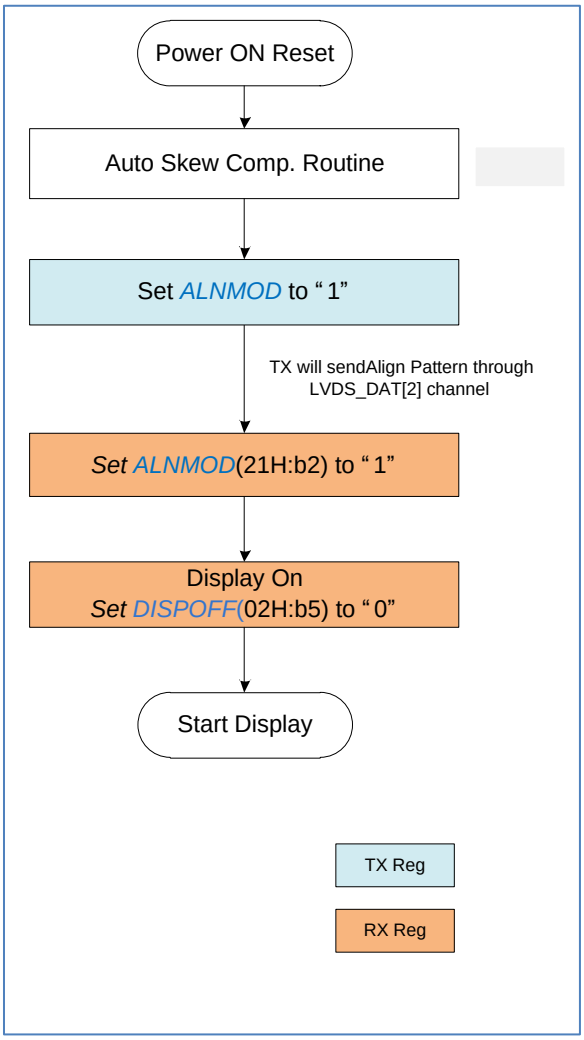
The Skew Compensation sequence is typically managed by a microcontroller and is performed before any data is sent to the display (The display's DISPOFF bit is set to "1" during this operation).



LVDS Alignment

This operation is performed at power on and at periodic intervals in order to maximize signal integrity and prevent spurious noise on the display. In the eMagin Design Reference Kit and the Verilog source code provided herein, this alignment is performed during every vertical blanking interval.

A flow chart of the LVDS Alignment operation is shown below:



The ALNMOD register is present in both the Transmitter (FPGA) and Receiver (Microdisplay) circuits.

Example RTL Code for LVDS_TXOUT_CTL.v

```
//-------------------------------------------------------------------------------------------------
//
// Title       : LVDS_TXOUT_CTL
// Design      : LVDS Tx Output Control Sample
// Author      : Jae Koh
// Company     : eMagin
//
//-------------------------------------------------------------------------------------------------
`timescale 1ns / 10ps

module LVDS_TXOUT_CTL ( HS_IN ,ALIGN ,rstn ,R_EV ,B_EV ,EN_IN ,EN_OUT ,vclk ,DOUT ,G_EV
        ,DE_IN ,VS_IN ,LVDSCTL ,VSPOL ,R_OD ,G_OD ,B_OD );

        input [7:0] R_EV ;              // Even Column Video Data
        input [7:0] G_EV ;
        input [7:0] B_EV ;
        input [7:0] R_OD ;              // Odd Column Video Data
        input [7:0] G_OD ;
        input [7:0] B_OD ;
        input vclk ;                    // Video Clock
        input EN_IN ;                   // Enable
        input VS_IN ;                   // VSYNC
        input HS_IN ;                   // HSYNC
        input DE_IN ;                   // Data Enable
        input rstn ;
        input VSPOL ;                           // VSYNC Polarity - 1:Positive, 0:Negative
        input [1:0] LVDSCTL ;           // {ALNMOD, SKWMOD}
        output EN_OUT ;                         // Enable Out
        output ALIGN ;                          // LVDS Signal Align Control
        output [63:0] DOUT ; // LVDS Data & CLK Out

        wire [7:0] R_EV ;
        wire [7:0] G_EV ;
        wire [7:0] B_EV ;
        wire [7:0] R_OD ;
        wire [7:0] G_OD ;
        wire [7:0] B_OD ;
        wire vclk ;
        wire EN_IN ;
        wire VS_IN ;
        wire HS_IN ;
        wire DE_IN ;
        wire rstn ;
        wire VSPOL ;
        wire [1:0] LVDSCTL ;
        wire EN_OUT ;
        wire ALIGN ;
        wire [63:0] DOUT ;

// Internal register define
        reg [64:0] DOUT0 ;
        reg [8:0] VSO;
        reg [4:0] ENO;
        wire ALGNO;
        wire ALNMOD = LVDSCTL[1] & ~LVDSCTL[0];
        wire SKWMOD = LVDSCTL[0];

        assign EN_OUT = ENO[4];
        assign ALGNO = VSO[0] & ~VSO[8] & ALNMOD;
        assign ALIGN = VSO[3] & ~VSO[6] & ALNMOD;
        assign DOUT = DOUT0;

        always @(negedge rstn or posedge vclk)
                if (!rstn)
                        begin
                                VSO <= 0;
                                ENO <= 0;
                                DOUT0 <= 0;
                        end
                else
                        begin
                                if (VSPOL)
                                        VSO <= {VSO[7:0], VS_IN};
                                else
                                        VSO <= {VSO[7:0], ~VS_IN};

                                ENO <= {ENO[3:0], EN_IN};

                                if (SKWMOD)
                                        begin
                                                DOUT0 <= 64'h0F0F0F0F0F0F0F0F;
                                        end
                                else
                                        begin
                                                DOUT0[63:56] <= 8'b01010101;            // LVDS_CLK
                                                //
                                                DOUT0[55] <= B_EV[5];
```

```
                                DOUT0[54] <= B_EV[4];
                                DOUT0[53] <= B_EV[3];
                                DOUT0[52] <= B_EV[1];
                                DOUT0[51] <= B_EV[0];
                                DOUT0[50] <= B_EV[2];
                                DOUT0[49] <= G_EV[7];
                                DOUT0[48] <= R_EV[0];
                                //
                                DOUT0[47] <= G_EV[6];
                                DOUT0[46] <= G_EV[5];
                                DOUT0[45] <= G_EV[1];
                                DOUT0[44] <= G_EV[0];
                                DOUT0[43] <= G_EV[4];
                                DOUT0[42] <= G_EV[3];
                                DOUT0[41] <= G_EV[2];
                                DOUT0[40] <= B_EV[7];
                                //
                                DOUT0[39] <= R_EV[7];
                                DOUT0[38] <= R_EV[1];
                                DOUT0[37] <= R_EV[6];
                                DOUT0[36] <= R_EV[5];
                                DOUT0[35] <= R_EV[4];
                                DOUT0[34] <= R_EV[3];
                                DOUT0[33] <= R_EV[2];
                                DOUT0[32] <= B_EV[6];
                                //
                                DOUT0[31] <= DE_IN;
                                DOUT0[30] <= DE_IN;
                                DOUT0[29] <= VS_IN;
                                DOUT0[28] <= VS_IN;
                                DOUT0[27] <= HS_IN;
                                DOUT0[26] <= HS_IN;
                                DOUT0[25] <= EN_IN;
                                DOUT0[24] <= EN_IN;
                                //
                                if (ALGNO)
                                        begin
                                                DOUT0[23] <= 1;
                                                DOUT0[22] <= 0;
                                                DOUT0[21] <= 0;
                                                DOUT0[20] <= 0;
                                                DOUT0[19] <= 0;
                                                DOUT0[18] <= 0;
                                                DOUT0[17] <= 0;
                                                DOUT0[16] <= 0;
                                        end
                                else
                                        begin
                                                DOUT0[23] <= B_OD[5];
                                                DOUT0[22] <= B_OD[4];
                                                DOUT0[21] <= B_OD[3];
                                                DOUT0[20] <= B_OD[1];
                                                DOUT0[19] <= B_OD[0];
                                                DOUT0[18] <= B_OD[2];
                                                DOUT0[17] <= G_OD[7];
                                                DOUT0[16] <= R_OD[0];
                                        end
                                //
                                DOUT0[15] <= G_OD[6];
                                DOUT0[14] <= G_OD[5];
                                DOUT0[13] <= G_OD[1];
                                DOUT0[12] <= G_OD[0];
                                DOUT0[11] <= G_OD[4];
                                DOUT0[10] <= G_OD[3];
                                DOUT0[9] <= G_OD[2];
                                DOUT0[8] <= B_OD[7];
                                //
                                DOUT0[7] <= R_OD[7];
                                DOUT0[6] <= R_OD[1];
                                DOUT0[5] <= R_OD[6];
                                DOUT0[4] <= R_OD[5];
                                DOUT0[3] <= R_OD[4];
                                DOUT0[2] <= R_OD[3];
                                DOUT0[1] <= R_OD[2];
                                DOUT0[0] <= B_OD[6];
                        end
                end

endmodule
```

14. APPENDIX C: EEPROM MEMORY MAP

Each WUXGA-R5 microdisplay contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I^2C serial interface that is used to communicate with the microdisplay. The device's serial address is as follows:

Write Mode: Address is A6h (or AEh if SERADD = 1) – *Prohibited mode*

Read Mode: Address is A7h (or AFh if SERADD =1)

The first 14 bytes (0x00 to 0x0E) represent identification codes of the WUXGA-R5 microdisplay. The following 93 (0x0F to 0x6C) bytes contain sequential data values that can be used to write to the microdisplay's internal registers starting with register address, "00h", to "39h".

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in yellow are measured at the factory and are specific to each individual device.

Memory Addr (hex)	WUXGA-R5 OLED Microdisplay
0	Serial Char #0
1	Serial Char #1
2	Serial Char #2
3	Serial Char #3
4	Serial Char #4
5	Lot Char#0
6	Lot Char#1
7	Lot Char#2
8	Lot Char#3
9	Lot Char#4
A	Lot Char#5
B	Wafer Char#0
C	Wafer Char#1
D	Wafer Char#2
E	Wafer Char#3
F	STAT
10	VINMODE
11	DISPMODE
12	LFTPOS
13	RGTPOS
14	TOPPOS
15	BOTPOS
16	ROWRESETL

17	ROWRESETH
18	RAMPCTL
19	Reserved
1A	RAMPCM
1B	VDACMX
1C	BIASN
1D	GAMMASET
1E	VCOM MODE
1F	VCM CTL
20	VGMAX
21	VCOM MODE
22	IDRF
23	DIMCTL
24	TREFDIV
25	TEMPOFF
26	TUPDATE
27	TEMPOUT
28	ANGPWRDN
29	SYSPWRDN
2A	TPMODE
2B	TPLINWTH
2C	TPCOLSP
2D	TPROWSP
2E	TPCOLOR
2F	DLYSEL
30	LVDSCTL
31	SKEW0_L
32	SKEW0_H
33	SKEW1_L
34	SKEW1_H
35	SKEW2_L
36	SKEW2_H
37	SKEW3_L
38	SKEW3_H
39	SKEW4_L
3A	SKEW4_H
3B	SKEW5_L
3C	SKEW5_H
3D	SKEW6_L
3E	SKEW6_H
3F	SKFAST
40	SKSLOW
41	SYNCMOD
42	LUT_ADDR
43	LUT_DATA_L
44	LUT_DATA_H
45	LUT_UPDATE

46	Reserved
47	Reserved
48	Reserved
49	Reserved
4A	Reserved
4B	Reserved
4C	Reserved
4D	Reserved
4E	Reserved
4F	Reserved
50	Reserved
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved
56	Reserved
57	Reserved
58	Reserved
59	Reserved
5A	Reserved
5B	Reserved
5C	Reserved
5D	Reserved
5E	Reserved
5F	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	Reserved
66	Reserved
67	NVCK0
68	NVCK1
69	Reserved
6A	Reserved
6B	Reserved
6C	Reserved
6D	VGNA0_HI
6E	VGNA0_LO
6F	VGNA1_HI
70	VGNA1_LO
71	VGNA2_HI
72	VGNA2_LO
73	VGNA3_HI
74	VGNA3_LO

75	VGNA4_HI
76	VGNA4_LO
77	VGNA5_HI
78	VGNA5_LO
79	VGNA6_HI
7A	VGNA6_LO
7B	VGNA7_HI
7C	VGNA7_LO
7D	VGNB0_HI
7E	VGNB0_LO
7F	VGNB1_HI
80	VGNB1_LO
81	VGNB2_HI
82	VGNB2_LO
83	VGNB3_HI
84	VGNB3_LO
85	VGNB4_HI
86	VGNB4_LO
87	VGNB5_HI
88	VGNB5_LO
89	VGNB6_HI
8A	VGNB6_LO
8B	VGNB7_HI
8C	VGNB7_LO
8D	GMMA00_HI
8E	GMMA00_LO
8F	GMMA01_HI
90	GMMA01_LO
91	GMMA02_HI
92	GMMA02_LO
93	GMMA03_HI
94	GMMA03_LO
95	GMMA04_HI
96	GMMA04_LO
97	GMMA05_HI
98	GMMA05_LO
99	GMMA06_HI
9A	GMMA06_LO
9B	GMMA07_HI
9C	GMMA07_LO
9D	GMMA08_HI
9E	GMMA08_LO
9F	GMMA09_HI
A0	GMMA09_LO
A1	MM
A2	DD
A3	YY

A4	YY