SXGA-120 R5

1280 X 1024 LOW POWER COLOR XL AMOLED MICRODISPLAY

DATASHEET

For Part Number:

EMA-101400-01

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eMagin Corporation 700 South Drive, Suite 201 Hopewell Junction , New York 12533 845-838-7900
www.emagin.com

Version	Date	ECN	Scope
-	05-17-2016	000002	Initial Release
A	03-01-2019	000693	Document cleanup, all sections
B	11-11-2019	000850	Updated power consumption (pp 12-14). Added spectrum in section 7 Corrected typos and clarified IDRF register description (Section 11.6)

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1. INTRODUCTION

The SXGA-120 R5 Color XL microdisplay from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high resolution, high image quality, compact size, and very low power. Combining a total of 4,015,536 active dots, the SXGA-120 display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

The SXGA-120 R5 is pin compatible with the EMA-100502-01 SXGA Color XL microdisplay but adds several new features including an improved power-on sequence that simplifies system design.

The active array is comprised of 1292 x 1036 square pixels with a 12-micron pitch and a 69% fill factor. An extra 12 columns and 12 rows (beyond the 1280 x 1024 main array) are provided to enable the active SXGA-120 R5 display to be shifted by steps of 1 or 2 pixels in the X and Y directions for optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 4 x 12 micron identical sub-pixels, which together form the 12-micron square pixel group. The backplane design allows for individual control of each of the 3 subpixels.

The SXGA-120 R5 design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. Video data is received via an extended 30-bit digital (10-bit per subpixel) interface with external synchronization and clocks, and the display includes on-chip digital to analog conversion, automatic luminance regulation over the full temperature range, gamma correction support, and programmable brightness.

The SXGA-120 R5 also includes a pulse-width-modulation (PWM) function that, together with the standard analog control (via the IDRF and DIMCTL registers), provides an extended dimming range. The PWM function also enables an impulse drive mode of operation that significantly reduces motion artifacts in high speed scene changes

The SXGA-120 R5 display system provides broad versatility and flexibility for the user through application of a separate FPGA driver IC or integration of drive logic into the user's electronics using eMagin provided source code. The driver IC provides control over gamma, contrast, brightness, electronic optical alignment, and video formatting.

Internal fault monitoring capabilities have been built into the SXGA-120 R5 design, that provide a means to inform the user via register and, optionally, a dedicated pin of specific internal faults. This option is not enabled on the standard product but can be special ordered (Part number: EMA-100406-01).

In addition, the SXGA-120 R5 display carrier board also includes a non-volatile memory component, accessible via the I2C serial bus. This component contains the preferred register settings for the SXGA-120 R5 microdisplay.

Detailed device specifications and application information for the SXGA-120 R5 XL microdisplay produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION – EMA-100400-01

2.1 EMA-101400-01 SXGA120 R5 Color XL Microdisplay

Parameter	**Specification[1]**
Display Type	Emissive, White Active Matrix Organic Light Emitting Diode on Silicon
Format	1280 (x3) x 1024 pixels
Total Pixel Array	1292 (x3) x 1036 pixels
Pixel Aspect Ratio	12 micron square group
Sub-Pixel Arrangement	Vertical Stripe (4 x 12 micron per sub-pixel)
Display Area	15.50 x 12.43 mm (19.87 mm diagonal, 0.78”)
Useable Display Area	15.36 x 12.29 mm (19.67 mm diagonal, 0.77”)
Mechanical Envelope	22.9 x 16.4 x 4.72 mm (rigid carrier board)
Weight	~ 2.5 grams
Gray Levels	256
Uniformity	≥ 85% end to end
Contrast Ratio	> 10,000:1 typical
Dimming Ratio	> 400:1 with CR> 1,000:1 typical
Luminance	≥ 150 cd/m2 (front luminance), SXGA 60Hz VESA mode
Video Interface	10-bit (x3, 1 channel per sub-pixel) Digital, 1.8 to 2.5V CMOS
Video Source Clock	135 MHz maximum (VESA mode), up to 85Hz frame rate
Control & Serial Interface	Digital 2.5V CMOS
Power Interface IO/Front-end Supply (VDD) Array/Analog Supply[2] (VAN) Bias Supply (VPG)	 2.5 Volts DC @ 10 mA maximum 5.0 Volts DC @ 200 mA maximum -1.5 Volts DC @ 1 nA maximum
Operating Ambient Temperature	-46ºC to +70ºC
Storage Temperature	-55ºC to +90ºC
Humidity	85%RH non-condensing

Note 1: The above data represents consumer and commercial performance specifications, measured at 20ºC, 60Hz frame rate and 150 cd/m2 luminance
Note 2: Includes internally generated negative cathode supply.

3. FUNCTIONAL OVERVIEW

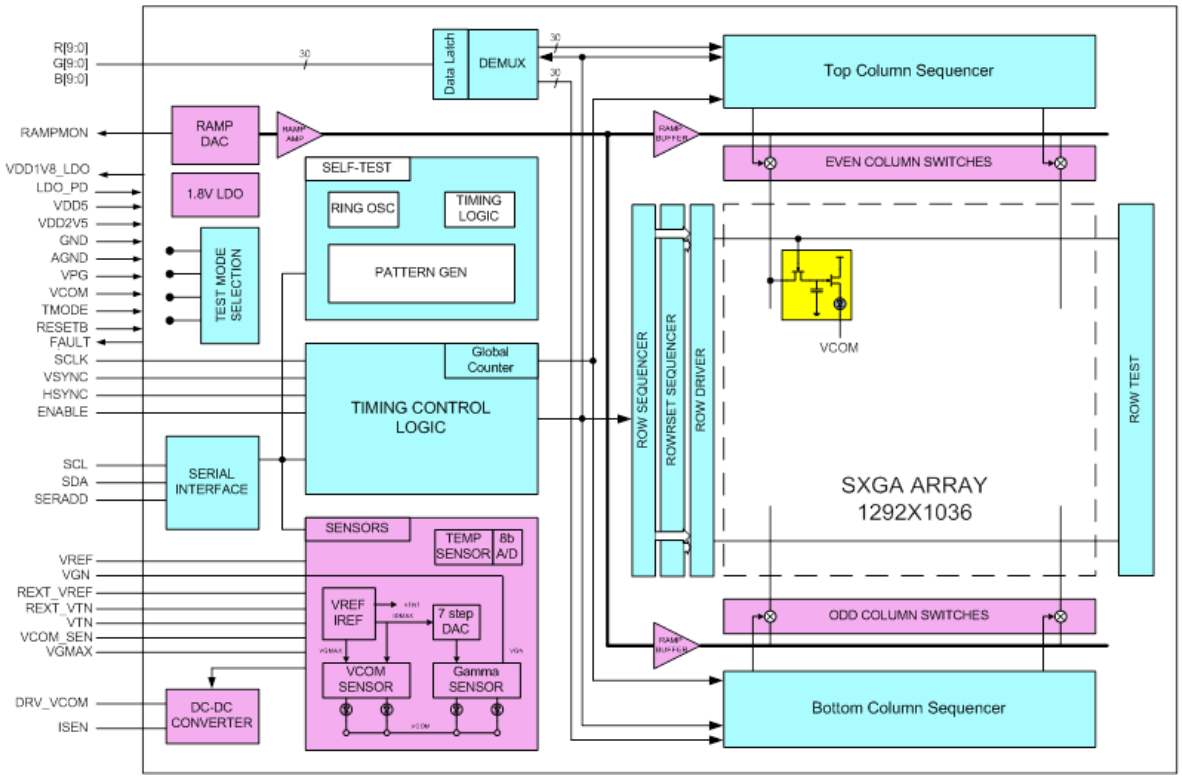


Figure 1 : SXGA-120 R5 Backplane block diagram

The top-level block diagram for the SXGA-120 R5 microdisplay is shown in Figure 1. Bi-directional row and column sequencer circuits are used for addressing individual cells within the 1292 x 1036 x 3 pixel array, and internal digital-to-analog conversion circuits are included for converting the digital input data into the analog signals needed for programming the pixels. A storage element (capacitor) resides at each pixel cell that is used to set the gray level.

The digital video input data is applied individually to each of the three RGB sub-pixels of the color group in color mode. The RGB data inputs that make up the digital data port are configured as three 10-bit data busses.

Odd columns are driven by data sequencers located at the top of the array and even columns by bottom side sequencers. To obtain a linear gray-scale response from the OLED pixels the digital input data must be formatted with Gamma correction.

The pixel clock and sync signals for various video formats are supplied externally and converted into individual control signals by the internal timing logic block. To simplify the external driving

requirements, several video formats are supported by the sequencer circuits including SXGA, HD720, and DVGA (in both progressive and interlaced modes).

The sensor block provides a number of signals for setting and regulating the display operation. These include a digital readout of the on-chip temperature, a reference level for maintaining constant luminance over temperature, a gamma correction feedback signal, and internal reference levels used for programming luminance over a wide dimming range.

An on-chip dc-to-dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the cathodes connected in common for all the array pixels via the VCOM input.

The 2-wire serial interface is a slave only I^2C compatible controller with a programmable address via an external pin (LSB). The interface provides access (read and write) to on chip registers. The registers will allow the display to be configured for its various video modes and associated clock parameters. Additional control settings include luminance control, image orientation and position, internal vs. external function selection, and various sensor settings.

The RESETB pin provides an asynchronous hardware reset function. When this pin is set to zero the display will turn off and the internal registers will be reset to their default state. After this pin is released (set to VDD) bit DISPOFF in register DISPMODE must be set high in order for the display to turn-on. If unused, this pin, which is connected to a weak internal pull up resistor, may be left unconnected.

The display also includes a built-in test pattern generator.

Table 3-1 : SXGA-120 R5 Microdisplay Video Formats

Format (columns x rows)	Name	Input Mode	Output (Display) Mode
1280 x 1024 Color	SXGA	Progressive Scan	Progressive Scan
1280 x 720 Color	HD720	Progressive Scan	Progressive Scan
640 x 480 Color	DVGA	Progressive Scan	Progressive Scan (Line and Pixel doubling)
1280 x 1024 Color	SXGA 3D	Frame Sequential	Frame Sequential 3D
1280 x 720 Color	HD720 3D	Frame Sequential	Frame Sequential 3D
640 x 480 Color	DVGA	Interlaced	Interlaced Scan (Line and Pixel doubling)

4. INPUT / OUTPUT DESCRIPTION

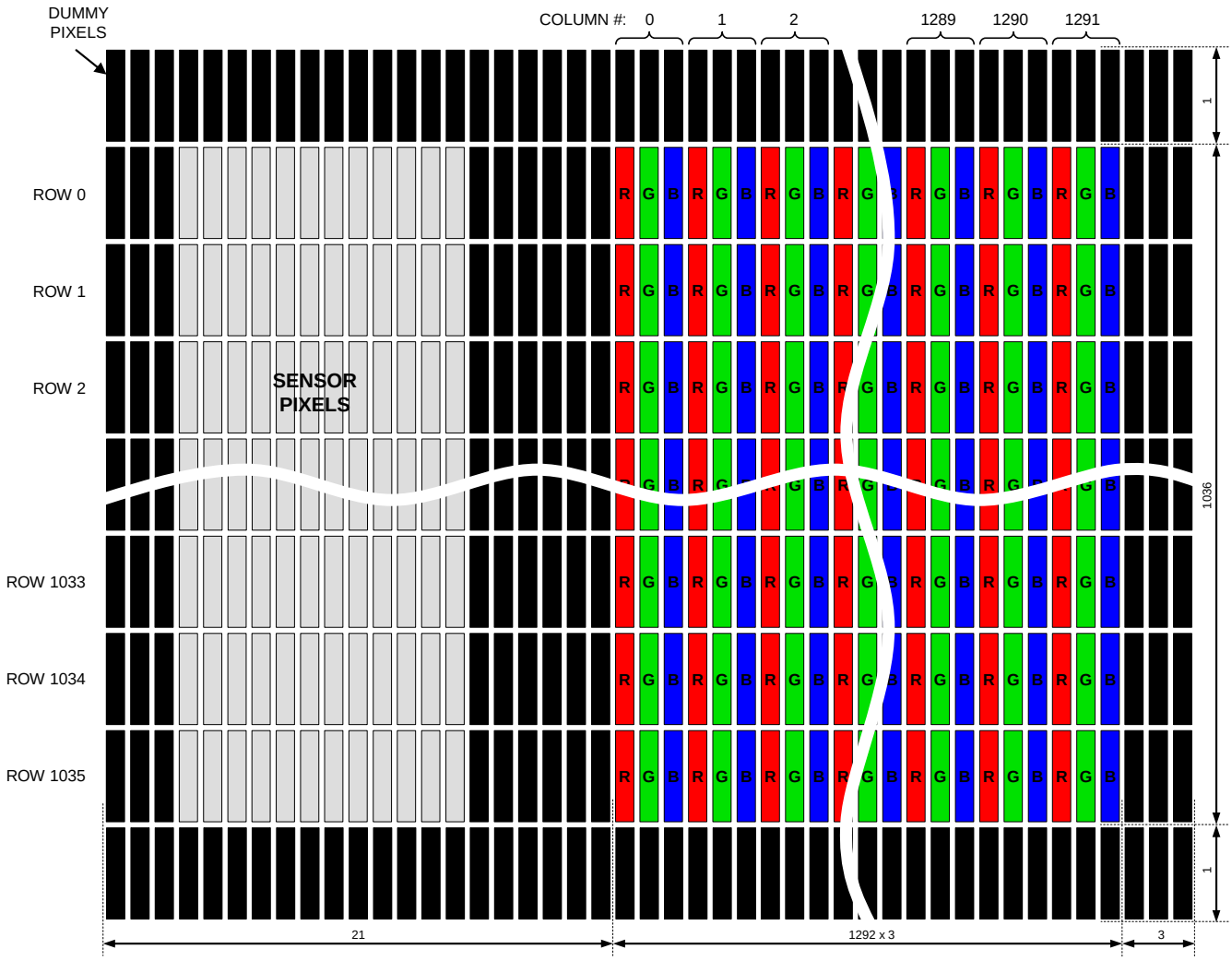
Miniature 50 pin header connector part number: Hirose DF12D(3.0)-50DP-0.5V(81)

Table 4-1 : Input / Output Pin Description

6/12/2009

Pin #	Pin Name	I/O	Signal Level	Description
1	VDD2.5	IN	Power	Logic and I/O power supply (2.5V)
2	VDD5	IN	Power	Analog and Array power supply (5V)
3	SCL	IN	Digital	Clock port for the serial interface (400 KHz Max)
4	VDD5	IN	Power	Analog and Array power supply (5V)
5	SDA	IN/OUT	Digital	Data port for the serial interface
6	GND	IN	Power	Power return terminal
7	SERADD	IN	Digital	Serial Interface LSB address bit. Must be connected. (2.5V CMOS)
8	GND	IN	Power	Power return terminal
9	RD0	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
10	VPG	IN	Power	Negative supply for array protection (-1.5V)
11	RD1	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
12	BI	IN	Digital	Burn In Mode selection pin. Active high. Internal pull-down. (2.5V CMOS)
13	RD2	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
14	VGN	OUT	Analog	Gamma sensor feedback signal (0 to 5V/2.5V analog output)
15	RD3	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
16	GND	IN	Power	Power return terminal
17	RD4	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
18	VSYNC	IN	Digital	Vertical Sync logic input. (2.5V CMOS)
19	RD5	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
20	HSYNC	IN	Digital	Horizontal Sync logic input. (2.5V CMOS)
21	RD6	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
22	DE	IN	Digital	Data Enable logic input used with loading RGB data. (2.5V CMOS)
23	RD7	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
24	GND	IN	Power	Power return terminal
25	RD8	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
26	SCLK	IN	Digital	Source clock input. (2.5V CMOS)
27	RD9	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
28	ENABLE	IN	Digital	Enable logic input. When inactive, blocks row and column sequencers. (2.5V CMOS)
29	GND	IN	Power	Power return terminal
30	RESETB	IN	Digital	Asynchronous System Reset. Active low. Internal pull-up. (2.5V CMOS)
31	BL0	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
32	GN9	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
33	BL1	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
34	GN8	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
35	BL2	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
36	GN7	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
37	BL3	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
38	GN6	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
39	BL4	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
40	GN5	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
41	BL5	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
42	GN4	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
43	BL6	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
44	GN3	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
45	BL7	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
46	GN2	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
47	BL8	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
48	GN1	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
49	BL9	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
50	GN0	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)

5. PIXEL ARRAY LAYOUT



The EMA-101400-01 is a color XL microdisplay. The picture above indicates how the input data maps onto the active array.

6. ELECTRICAL CHARACTERISTICS

Table 6-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	-0.3		2.75	VDC
VAN	Array Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3		0	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-35		+125	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 6-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	2.375	2.5	2.625	VDC
VAN	Array Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-46	+25	+70	°C
Pdt	Power Consumption		200	900(1)	mW

Note (1): With registers IDRF = 0xD8, DIMCTL = 0x64 and VGMAX = 0x0D

Table 6-3 : DC Characteristics

(Ta = 25°C, VDD =+2.5V, VAN = +5V, GND = 0V)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply		2.5		V
VAN	Array Power Supply		5		V
VCOM	Common electrode bias	-5	-2.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		1	V
Vih	Digital input high level	1.8		VDD+0.3	V
Vol	Digital output low level			0.5	V
Voh	Digital output high level	2.4			V
Vsl	Hsync, Vsync input low	GND-0.3		1	V
Vsh	Hsync, Vsync input high	1.8		VDD+0.3	V
VGN	Gamma feedback signal	0		2.5	V
	Variability	4	30	50	%
	Output Impedance		150		Ohm
	Peak Output Current			6	mA
Ipix	Average Pixel Current per frame	0	6	15	nA
Ipix_inl	Average Pixel Current Integral Non Linearity			5	%
Ipix_dnl	Average Pixel Current Differential Non Linearity			1	%

Table 6-4 : AC Characteristics

Ta = +20°C, L = 150 cd/m^2, 60Hz refresh rate,
GND = 0V, VDD= +2.5V, VAN = +5.0V,VPG = -1.5V

Symbol	Parameter	Min	Typ.	Max.	Unit
SCLK	Video Clock Frequency	12	-	135	MHz
CLK_Duty	SCLK duty cycle	40		60	%
Fhs	Horizontal Sync frequency	15.734		80	KHz
Fvs	Vertical Sync Frequency	30		85	Hz
Tlo	Line Overscan (% of line time)	3			%
Tfb	Frame Blanking (% of frame time)	1			%
Trst	Reset Pulse Width	100		-	µs

Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VAN	Average Van Power Consumption (SXGA Mode 60 Hz refresh rate)		160		mW
Pd VDD	Average VDD Power Consumption (SXGA Mode 60 Hz refresh rate)		18		mW
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode*		2.5		mW
Ta	Ambient Operating Temperature	-46		+70	°C

*Note: Input data, sync and clock lines must be inactive and held low

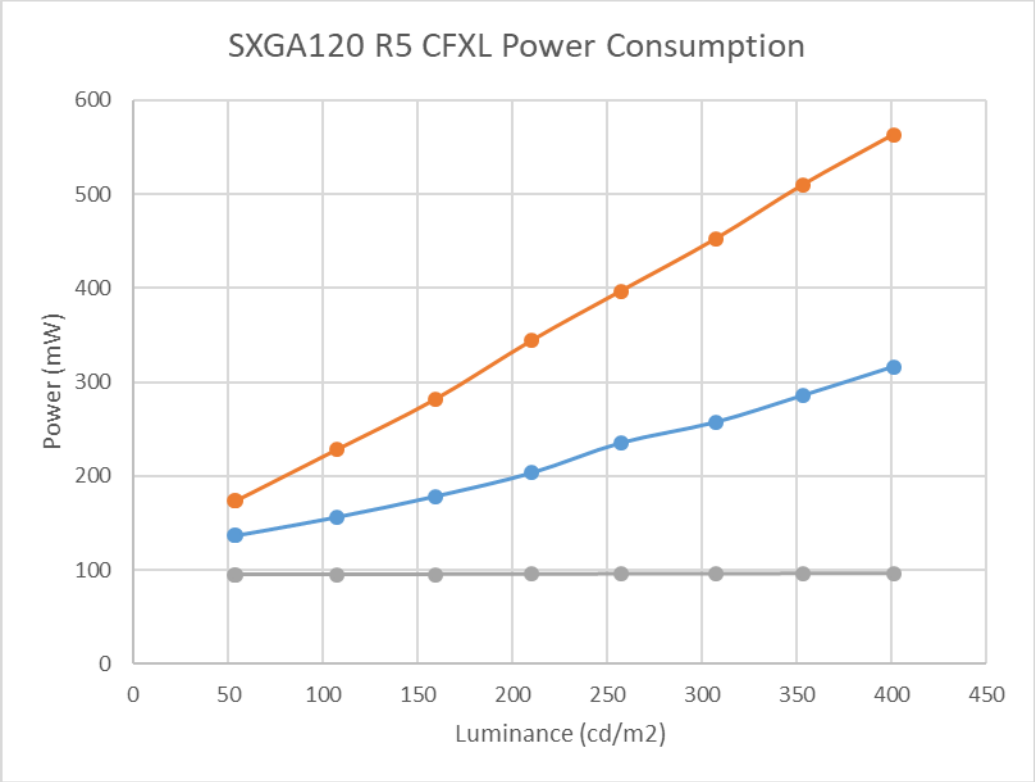
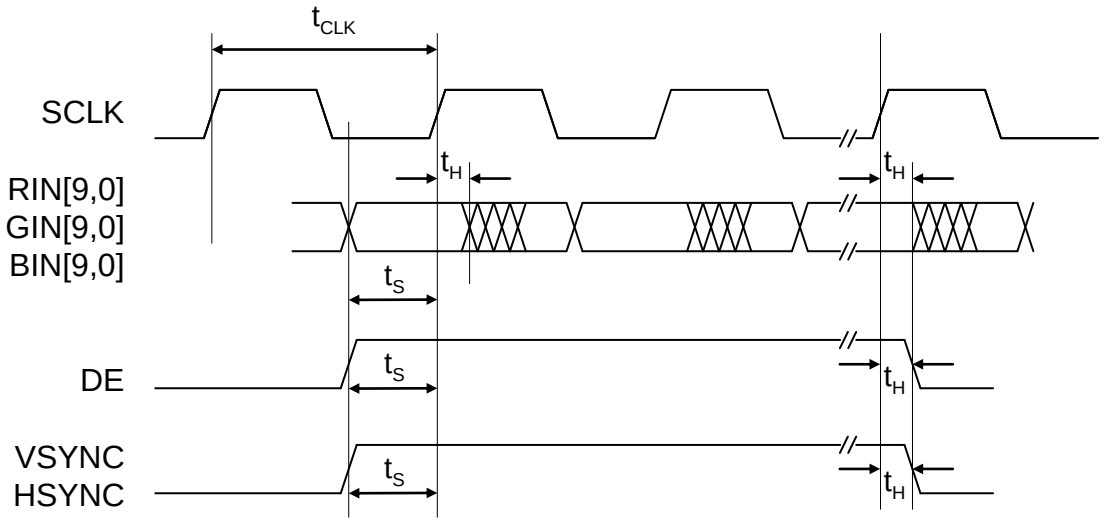
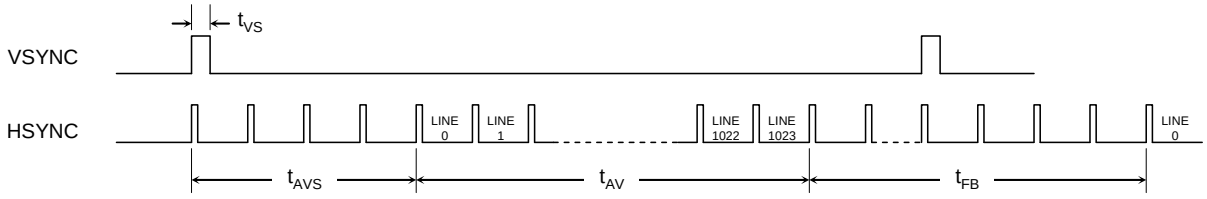


Figure 2 : Total power consumption vs. luminance at 20ºC – SXGA-120 R5 CFXL

6.1 Timing Characteristics

6.1.1 Interface Timing Diagrams





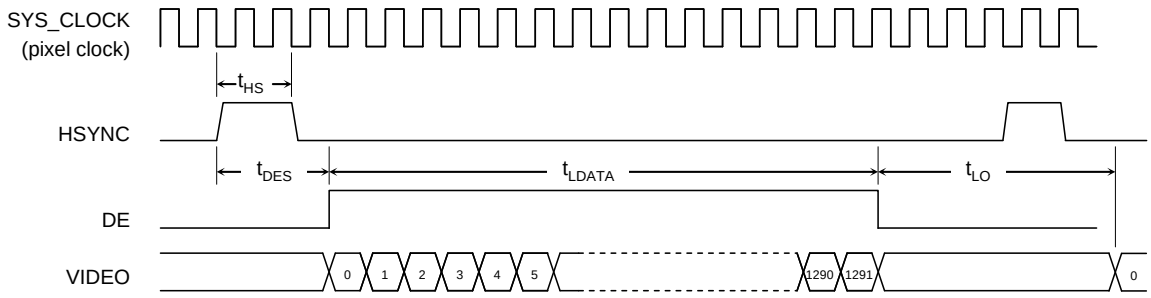
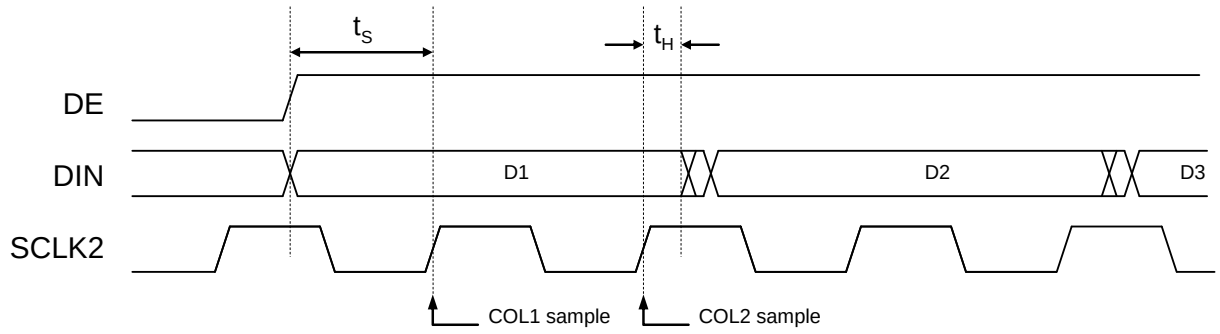


Table 6-5 : Input Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Video Input Setup/Hold (RIN/GIN/BIN)	t_S	4			ns
	t_H	1			ns
Control Signals Setup/Hold (DE/HSYNC/VSYNC)	t_S	4			ns
	t_H	1			ns
Clock Frequency	f_{CLK}		108[1]		MHz
Clock Period	t_{CLK}		9.26		ns
Clock Duty	D_{CLK}	40		60	%
VSYNC Pulse Width	t_{VS}	3			Hsync period
Time to Active Video Start	t_{AVS}	4			Hsync period
Frame Blanking (% of frame time)	t_{FB}	1			%
HSYNC Pulse Width	t_{HS}	4			SCLK period
Time to DE Start	t_{DES}	12			SCLK period
Line Overscan (% of line time)	t_{LO}	3			%

Note 1: SXGA @ 60Hz frame rate

6.1.2 DVGA Mode Timing Diagram



6.1.3 Gamma Sensor Timing Diagram

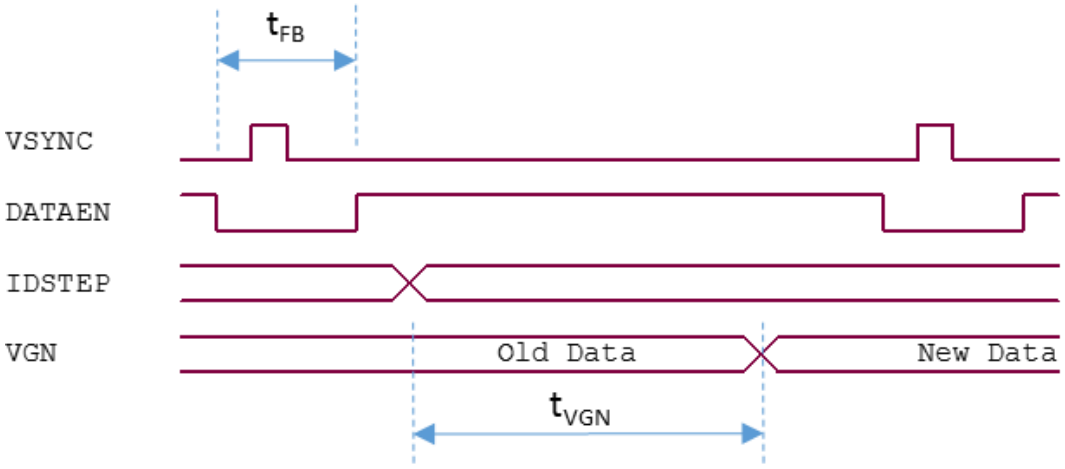


Table 6-6 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	1			%

Note: t_{VGN} is smaller than 10ms for higher IDSTEP values

7. OPTICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level	0.35	140	400	cd/m^2
	Variability	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE White	CIE-X	0.270	0.300	0.340	
	CIE-Y	0.320	0.360	0.380	
CIE Red	CIE-X	0.570	0.620	-	
	CIE-Y	0.290	0.340	0.370	
CIE Green	CIE-X	0.210	0.290	0.320	
	CIE-Y	0.450	0.510	-	
CIE Blue	CIE-X	-	0.140	0.190	
	CIE-Y	-	0.115	0.170	
GL	Gray Levels Per Color	256		1024	levels
F_R	Refresh Rate	30		85	Hz
FF	Emissive Area/Total Sub-pixel Area		0.69		
U_{LA}	End to end large-area uniformity	85(1)			%
S_{VH}	Pixel spatial noise at ½ luminance (1STD)			5	%
S_{LOT}	Peak-to-peak luminance variation over operating temperature range			8	%
T_{ON}	Time to recognizable image after application of power			0.5	sec

Table 7-1 : SXGA-120 R5 Color XL Microdisplay Optical Characteristics

Conditions: Ta = +20ºC, VDD = +2.5V, VAN = +5V, VPG = -1.5V, VCOM = internally generated, 100% PWM duty, L = 150 cd/m^2

Note 1: At 100% of gray level brightness and 100 cd/m2 luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display. 5 rectangular boxes are displayed (center and four corners) and driven to 1000 cdm^{-2}, the rest of the display is driven to black. A luminance

measurement is taken over the approximate center of each box. The Uniformity is defined as Lmin/Lmax in %

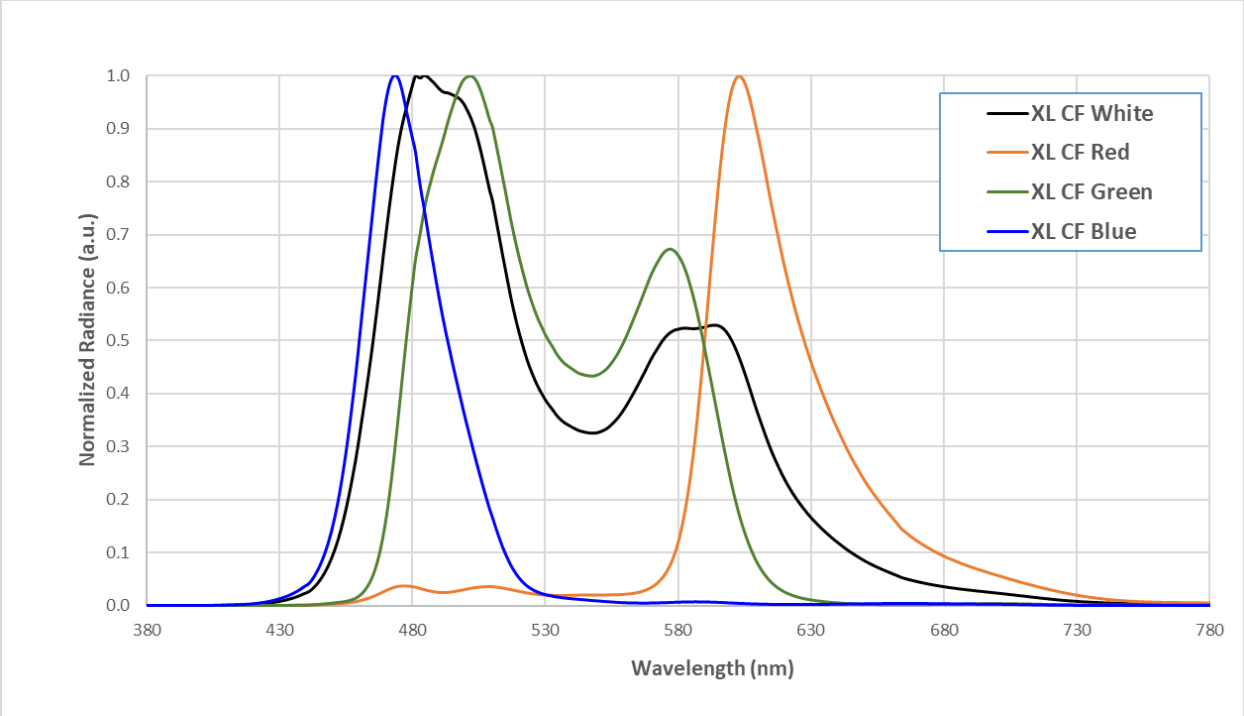


Figure 3: Normalized Spectrum (White, R, G and B)

8. MECHANICAL CHARACTERISTICS

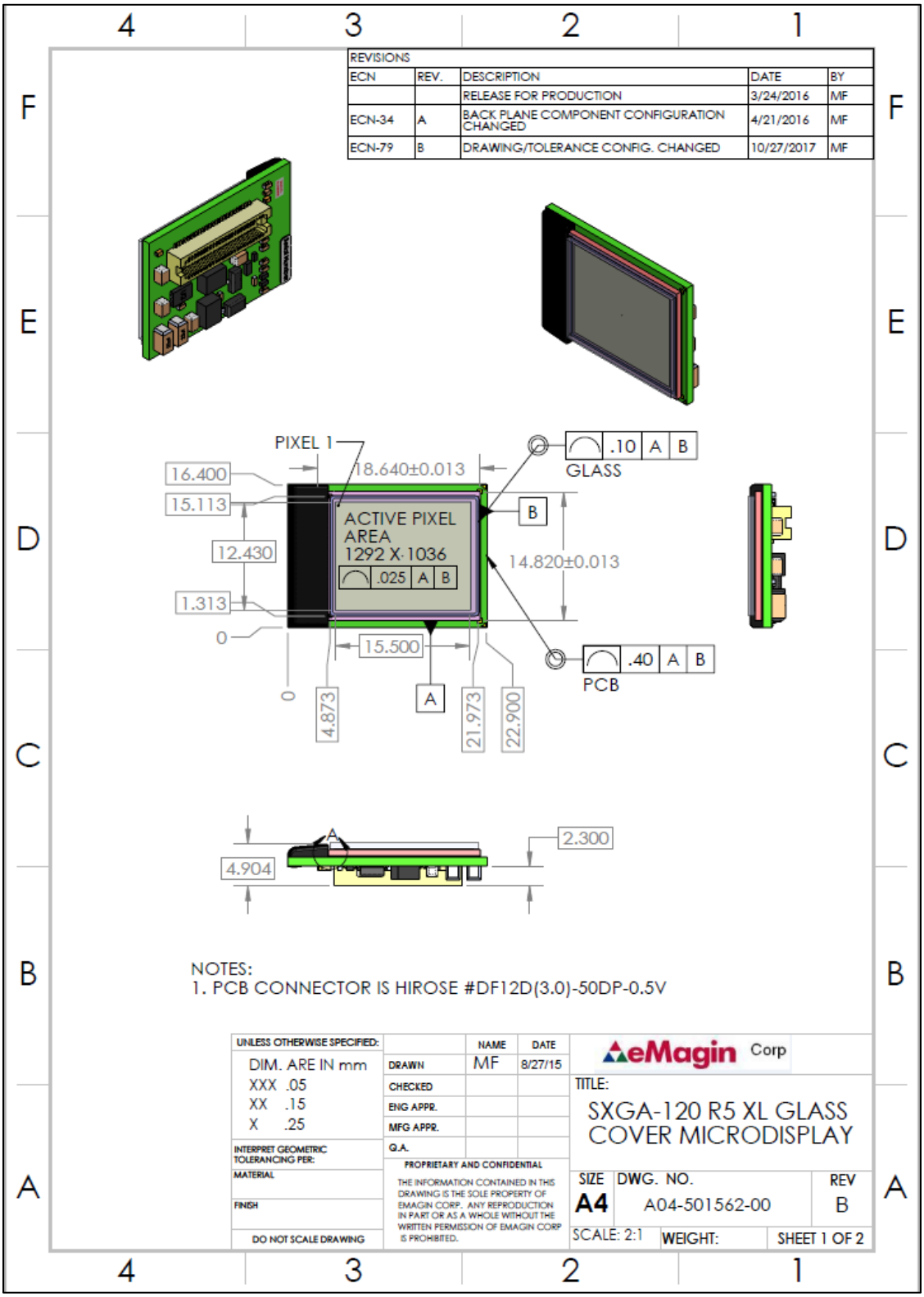
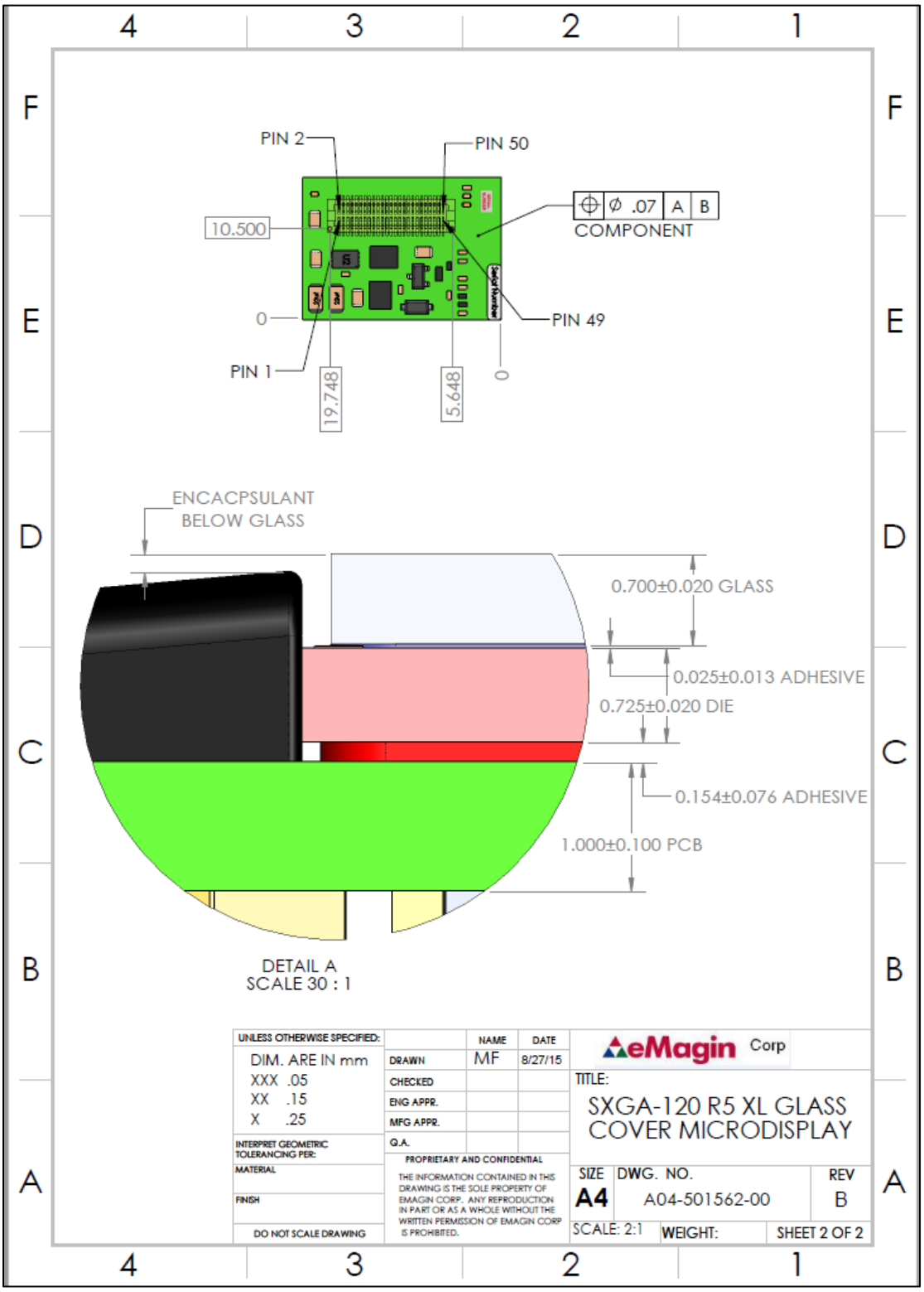


Figure 4: SXGA-120 R5 Assembly Drawing with 0.7mm Glass Cover (A04-501562-00)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Ø .07 A B
COMPONENT
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PIN 49
PIN 1
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5.648
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ENCACPSULANT
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0.025±0.013 ADHESIVE
0.725±0.020 DIE
0.154±0.076 ADHESIVE
1.000±0.100 PCB
DETAIL A
SCALE 30 : 1
UNLESS OTHERWISE SPECIFIED:
DIM. ARE IN mm
XXX .05
XX .15
X .25
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING
NAME
DATE
DRAWN
MF
8/27/15
CHECKED
ENG APPR.
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eMagin Corp
TITLE:
SXGA-120 R5 XL GLASS COVER MICRODISPLAY
SIZE
A4
DWG. NO.
A04-501562-00
REV
B
SCALE: 2:1
WEIGHT:
SHEET 2 OF 2

Connector J1

Manufacturer:	Hirose
Manufacturer Part Number:	DF12D(3.0)-50DP-0.5V(81)

Mating Connector Information

Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-50DS-0.5V(81)

Weight:	< 2.5 grams
Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.3 mm (both axes)

Flame Resistance Information

- Printed Circuit Board UL94V-O
- Connector UL94V-O
- Wirebond Encapsulant Flammability: 1 Flash point: 93°C
- Cover Glass Non flammable
- Silicon IC Non flammable

9. CLEANING HANDLING AND STORAGE RECOMMENDATIONS

9.1 Cleaning

When cleaning the displays we recommend the use of TECH-SPEC lens cleaner, manufactured by Edmund Optics Inc. and Alpha wipes 1010

The use of diluted IPA is also approved for cleaning the display. Care must be taken to ensure no residue remains after wiping the display surface

9.2 General handling considerations

- Do not expose the display to strong acids, bases, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation
- Temperatures in excess of the specified operating and storage range can cause irreversible damage to the display.
- Do not allow sharp objects to contact the exposed regions of the silicon display chip.
- Avoid immersion of the display in any liquid.
- The glass cover slip protects the display surface from most forms of damage and may be cleaned using techniques appropriate for fine lenses.
- Avoid applying force to the glass relative to the display chip in compressive, tensile, and sheer directions.

Figure 5: Best method of handling the displays

Figure 6: Avoid this method of display handling

9.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge damage. The following measures are recommended to minimize ESD occurrences:

- When handling the microdisplay, operated under a flow of ionized air to discharge the panel
- Use a conductive wrist strap connected to earth ground via a 10 M-Ohm resistor.
- Wear non-chargeable clothes
- Keep stored displays away from charged materials

9.4 Protection from Dust and Dirt

It is also recommended that all display handling operations take place in a clean environment. The use of ionized nitrogen gas is the preferred method of removing particles from the surface.

9.5 Short Term Storage

For short term storage (one to two weeks or less), the displays should be kept in their original container at room ambient and the typical controlled office environment.

9.6 Long Term Storage

For displays that will be stored for a longer period (a few weeks and up), it is recommended to keep displays stored in a dry environment near or at room ambient (20ºC typically) whenever possible prior to installation into an optical subsystem.

There are several ways to achieve this:
- Dry storage cabinet
- Dry Nitrogen cabinet
- Nitrogen sealed bag
- Vacuum sealed bag with desiccant

9.7 System Integration

Care must be taken when attaching the SXGA microdisplay to a housing. Specifically, there should be no contact between the top of the silicon die and any surface: the glass cover is the only approved surface that can be in contact with a housing cover on the front side of the microdisplay. The rear side of the circuit board assembly (where the connector is) can be used with adhesives to attach to a frame or housing.

The use of Super-X adhesive to attach the SXGA microdisplay to a frame or housing is approved.

10. DETAILED FUNCTIONAL DESCRIPTION

10.1 Video Input Interface

The 30-bit digital input port is comprised of three 10-bit data busses that make up the RGB data inputs. Separate synchronization signals (VSYNC and HSYNC) and the pixel clock (SCLK) are to be provided by the external video source. The data valid signal (DE) is used to signal the start of loading a row of data into the internal line memory. An active ENABLE signal is required for the Stereovision mode (inactive for all other modes, except Interlaced Video). The timing diagram for the input data bus is shown in Figure 7.

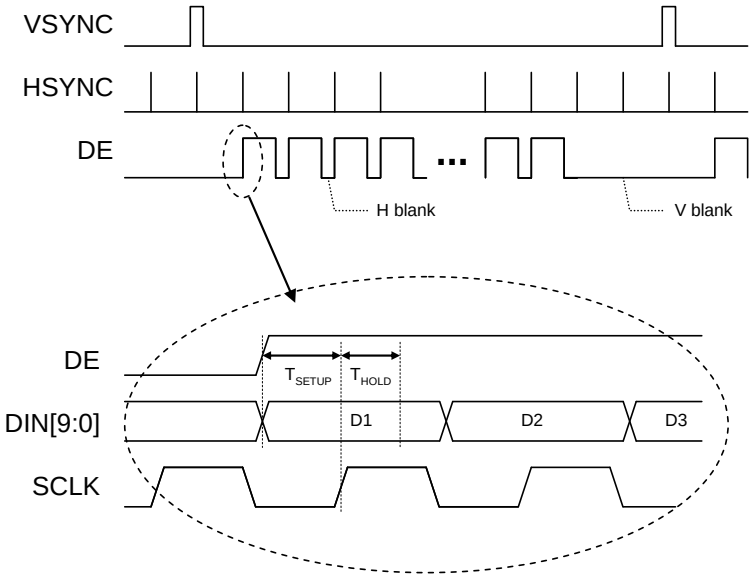


Figure 7 : Input Data timing diagram.

The input data to the display requires certain formatting that must be applied by the external drive electronics as described below.

10.1.1 Gamma Correction

Due to the non-linear electro-optic characteristic of the OLED pixel, a gamma correction signal must be applied to the video input signal to achieve a linear system response for the display. Since the optimum gamma curve will vary with temperature and luminance, it should also be regularly updated to account for changes in operating conditions. The color balance for the display can be modified by controlling the gamma individually for each of the three color data channels. Figure 8 illustrates the behavior of different components of the SXGA display system. The OLED response curve shown in the figure is an example of the typical optical response to

input data of the microdisplay and demonstrates its highly nonlinear characteristic. The Gamma Correction function shown in the figure is obtained by inverting the OLED response function. As demonstrated by the measured system response curve in the figure, the overall system display response becomes linear when the source video data is modified by the Gamma Correction function before being applied to the SXGA.

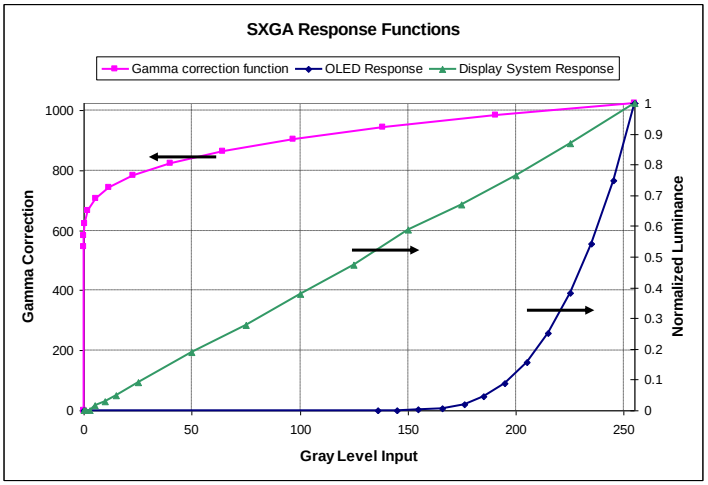


Figure 8: Gamma corrected system response characteristic

As shown in Figure 9, a typical SXGA application will include a 256x10-bit look-up-table for each color channel located in the data path between the video source and the display. The LUT, which is contained in an external FPGA, converts the 8-bit data byte for each color of the video source into a 10-bit output data word for driving the microdisplay. The LUT is programmed with the gamma correction function required to linearize the system for the current operating conditions. Due to the non-linear characteristic of the OLED display, a 10-bit input to the SXGA is used to ensure a linear 8-bit optical response with better than 1-lsb accuracy. The LUT data must be in Gray Code format as described in section 10.1.2.

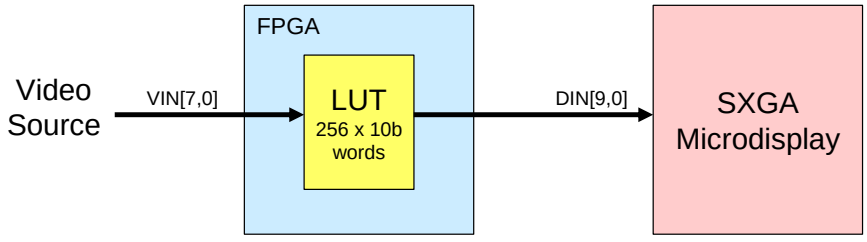


Figure 9: Gamma correction using a look-up-table (LUT)

On-chip support for generating the gamma correction function in the form of an 8-segment piecewise-linear function is described in section 10.4.7. A total of 8 data points (Q1…Q8) that lie on the gamma curve as shown in Figure 10 are provided by the display chip while point Q0 is a fixed value set by the user. The external microcontroller can use this information to generate intermediate data points for the entire 256 point curve by linear interpolation.

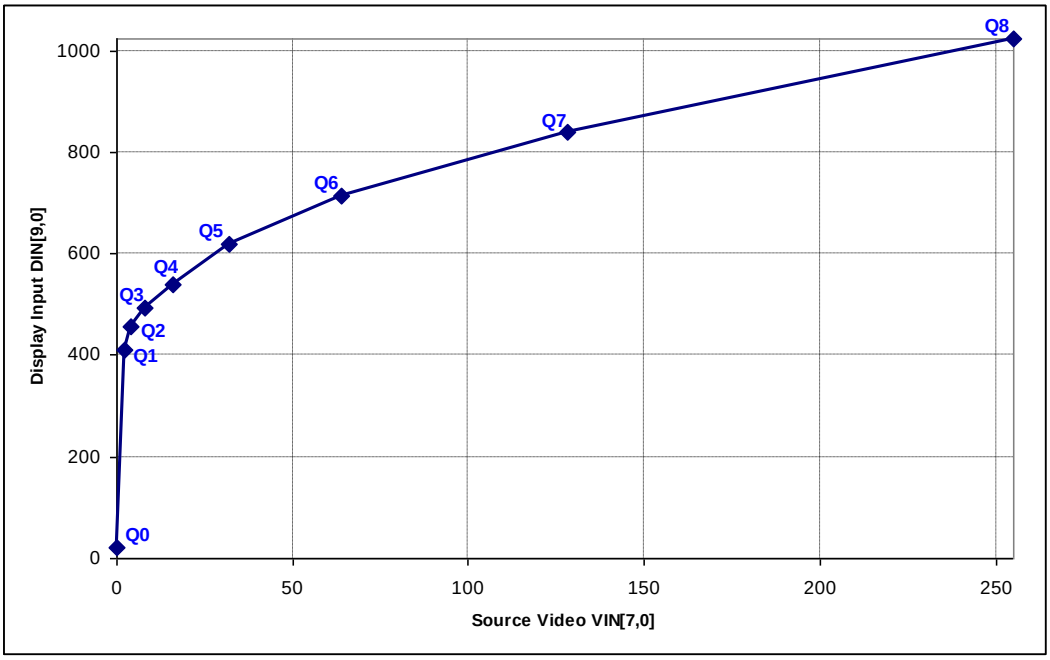


Figure 10: Typical SXGA gamma correction function

10.1.2 Gray Code Format

Input data to the SXGA digital port must be in Gray Code format to match the gray-code global counter used in the display chip. The conversion is carried out on each 10-bit color vector by the external drive electronics according to the following relationships:

G[0] = B[0] XOR B[1]
G[1] = B[1] XOR B[2]
G[2] = B[2] XOR B[3]
G[3] = B[3] XOR B[4]
G[4] = B[4] XOR B[5]
G[5] = B[5] XOR B[6]
G[6] = B[6] XOR B[7]
G[7] = B[7] XOR B[8]
G[8] = B[8] XOR B[9]
G[9] = B[9]

where G[9,0] is the 10-bit Gray word corresponding to the 10-bit binary word B[9,0].

10.1.3 Row Data Expansion

Since the display is comprised of 1292 column lines, the external drive electronics should add 12 dummy pixels with black data to each row of 1280 pixels provided by the source signal. The dummy pixels can be distributed between the start and end of the row data according to the desired horizontal location of the active window within the pixel array.

10.2 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

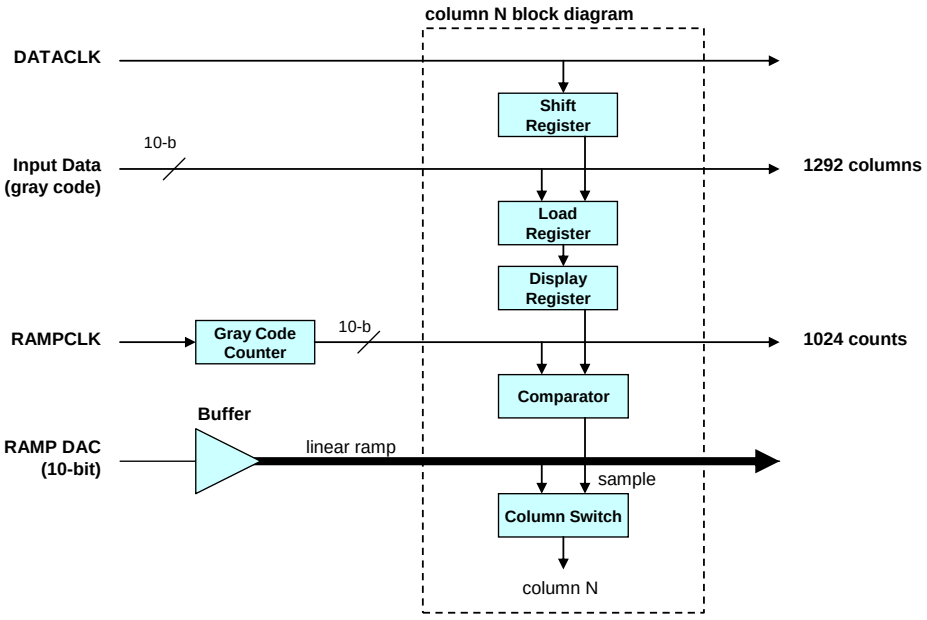


Figure 11 : Data sampling for Column N

A block diagram of one column drive circuit is shown in Figure 11. The 1292 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally

supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

A timing diagram for the data sampling process is shown in Figure 12. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VAN rail after 1024 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via register bits 4 & 5 (RAMPDLY2) in the RAMPCTL register (05h), its peak value can be set using register DAOFFSET, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

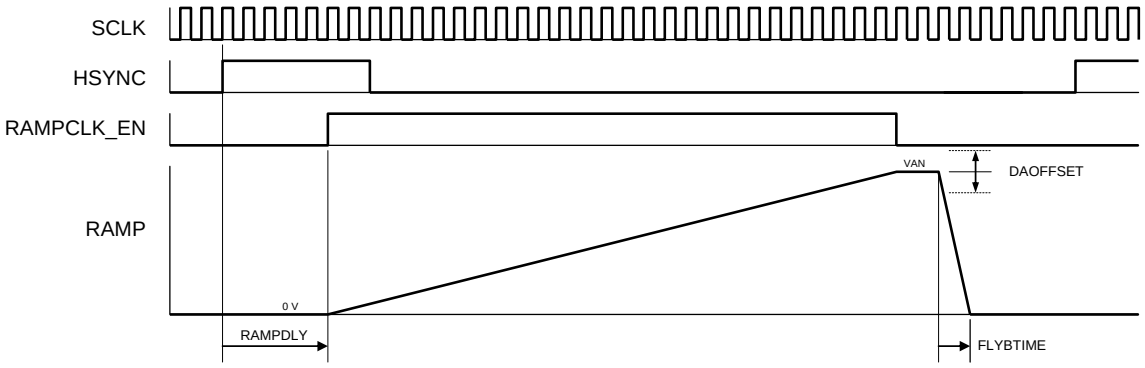


Figure 12 : Timing diagram for column data sampling

10.3 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, TOPPOS, and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before the display lights up.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

Selection among the main supported display formats is done via register bits RESOLUTION, TOPPOS, BOTPOS, and the external drive electronics. Bit RESOLUTION in the DISPMODE register is used to set the counter that defines the number of active video rows to be either 1024 (default), 720 or 960 (line doubled). For resolutions lower than the native resolution the inactive rows are driven to black. In the 960 mode (DVGA), used for VGA input format only, both the line doubling feature, where each line of data drives a row-pair, and the pixel-doubling feature, where each pixel is written into a column-pair resulting in 1280 visible pixels, are activated. In DVGA mode the SCLK provided by the drive electronics must run at double the frequency of the video source clock for pixel doubling to be achieved.

The starting row is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in SXGA mode is vertically centered in the array. These registers allow the active window to be shifted vertically in 1 line steps by up to ±6 lines in the SXGA mode and up to ±255 lines in HD720 mode. In DVGA mode the active window can be shifted in 2 line steps by up to ±38 lines.

The starting column is determined by the external drive electronics which must add 12 dummy black pixels to each row of incoming data as described previously. This allows the active window to be horizontally shifted in 1 pixel steps by up to 12 pixels total.

10.3.1 Interlaced Mode

Bit SCMODE in the DISPMODE register is used to select either progressive or interlaced mode for all formats. By default (SCMODE=0) the normal progressive mode is active. Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field. In the case of interlaced VGA format, automatic line doubling is activated in which the shift register drives sequential pairs of rows. Figure 13 shows the interlace option for VGA with row doubling.

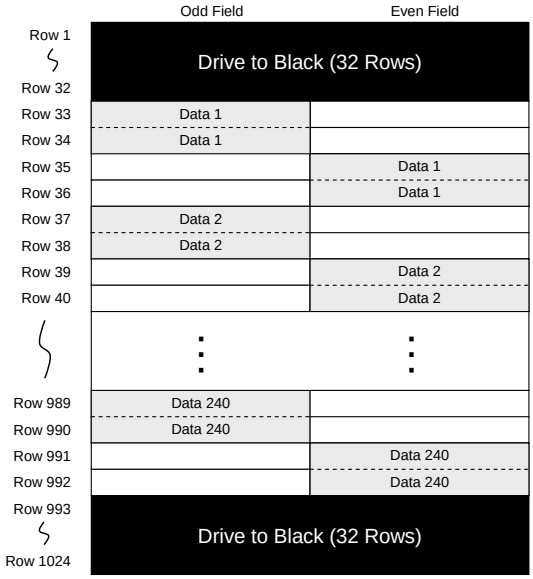


Figure 13 : Interlace option showing VGA mode with line doubling

Field status in interlaced mode is provided via the ENABLE input pin. The state of this pin is latched on the falling edge of VSYNC. When register bit SET_FIELD = “0” then a logic low at the ENABLE pin indicates that Field 1 (odd field) is active, and a logic high indicates that Field 2 (even field) is active. The opposite states are indicated when SET_FIELD is set to 1.

10.3.2 Stereovision

The SXGA is designed with binocular stereovision applications in mind. As a result of the fast OLED response time and the presence of a storage capacitor at each pixel, the microdisplay can operate at low refresh rates without showing flicker.

This will allow the displays to be used with a frame or field sequential (more generally known as time sequential) stereovision mode using a single video input channel, and therefore providing a simple means to leverage the capabilities of PC compatible computers using stereo compatible graphics adapters, such as the Nvidia GeForce series. The frame sequential stereovision mode supported should follow the Video Electronics Standards Association (VESA) Connector and Signal Standards for Stereoscopic Display Hardware. This standard is available from VESA at www.vesa.org.

The ENABLE input pin will allow for a direct implementation of the VESA standard without additional external components. The microdisplay can be programmed for either an active high or low Enable, allowing a single signal to be used with two displays. In such a configuration, one display scans and displays while the other one holds and displays.

The ENABLE input acts, when set low, as a mask for HSYNC and VSYNC. It does not blank the display but prevents it from acquiring another frame of data until released. This is a real time input. The active state (high or low logic level) is programmed by the SET_ENABLE bit in the VINMODE resister.

The 3D-MODE bit of the DISPMODE register will be used to set either the Stereovision mode of operation (1) or Normal (non-3D) operation (0).

Frame Sequential Mode:
In Time Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE=”1” the SCMODE bit in the DISPMODE register is set to Progressive Scan Mode (00H) for frame sequential mode. The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard mentioned above, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The stereovision mode is controlled by both the Enable input pin and by the SET_ENABLE bit of the VINMODE register. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value will be used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= “0”). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display must be configured with Enable active high (SET_ENABLE=”1”). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source). This is illustrated by the timing diagram shown in Figure 14.

Line Interleaved Mode:
In Line Interleaved Mode each video frame contains information for both the left and right eyes. Consequently, the resolution is reduced in half for each display but they both run at the full frame rate. The operation of the Enable input pin and the SET_ENABLE bit will be similar to Frame Sequential Mode except that now the Enable input toggles at the line rate.

For non-3D-Mode operation, the SET_ENABLE bit can be set to either 0 (logic low) or 1 (logic high), and the Enable pin input needs to be tied to VDD (2.5V).

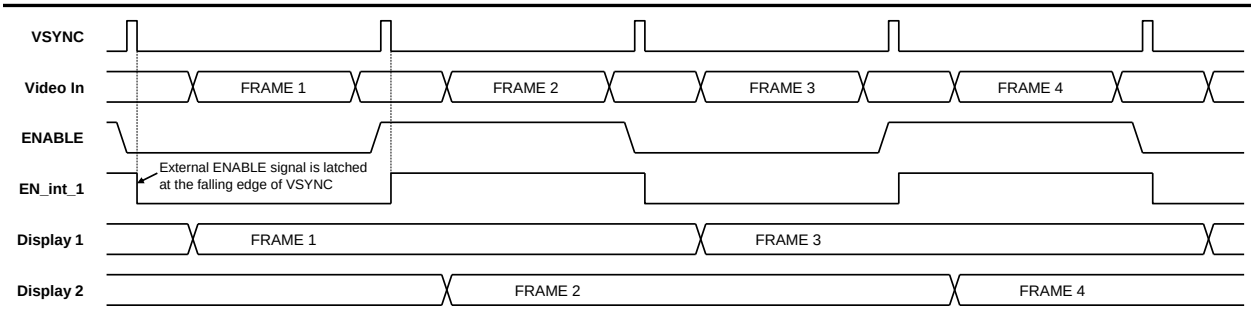


Figure 14 : Timing for frame sequential stereovision mode

10.3.3 Row Duty Rate Control

The duty rate for a row of data is defined as the fraction of a frame period during which the pixels maintain a programmed value; for the remainder of the frame period the pixels will be driven to black.

A Row Reset function is provided in the SXGA120 R5 to allow the duty rate of rows to be controlled between 0 and 100% (default condition). The register ROWRESET[9,0] is used to set the number of Hsync cycles during which the pixel data remains in the on-state, during a frame period. For ROWRESET=0 the pixel data is never driven to black and the duty rate for pixel data is equal to 100% (default). For ROWRESET=W the pixels in any row are driven for 2*W Hsync cycles in an active frame period, and turned to black for the remainder of the frame time.

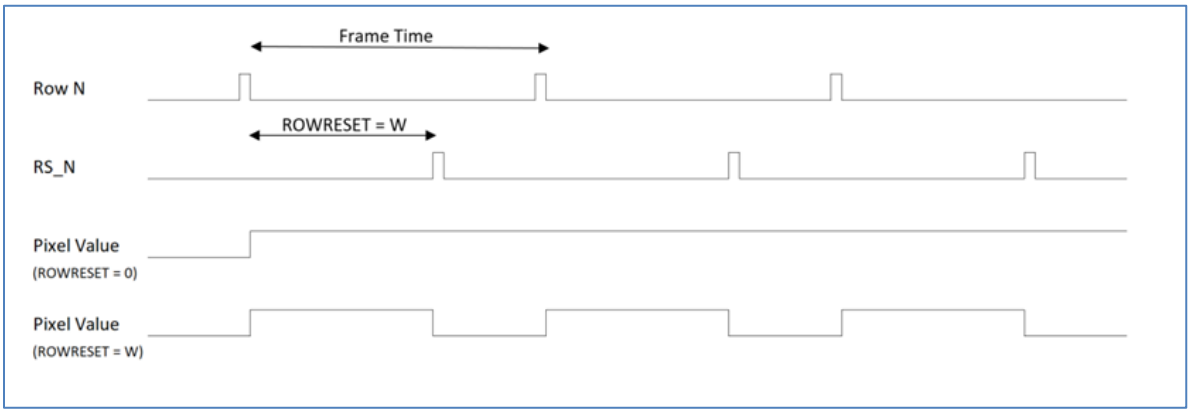


Figure 15: Timing diagram showing Row Reset functionality

The operation of the Row Reset function is depicted in the timing diagram shown in Figure 14. All the pixels contained in ROW N are programmed during the (Nt+1)th horizontal line scan following the initialization line scans which occur at the beginning of a video frame. Normally this pixel data is stored in the pixel and remains unchanged until it is refreshed during the next frame

period. When the Row Reset function is activated, the pulse RS_N is generated at a position determined by the value of register ROWRESET. For example, when the register value is equal to W the rising edge of RS_N occurs exactly 2*W Hsync cycles prior to the next programming cycle for ROW N. The pulse RS_N sets all the pixels in ROW N to black until the next programming cycle. All rows in the array will operate at the same duty rate. As a result the duty rate for all the rows in the pixel array will be given by

$$ROW\_DUTY = \frac{2 * W * T_{HSYNC}}{T_{FRAME}}$$

This function can be used to control dimming (see section 9.4.5) to extend the display dimming range. A side benefit of this function, when used for dimming, is that no gamma update is needed when dimming is done exclusively with the Row Reset function.

Another use of this function is to reduce motion artifacts: the net visual effect of limiting the on-time of a given row is a reduction in visual persistence. This allows the eye to "forget" the state of the row prior to its update with potentially new information, and leads to the perception of a smoother motion when an object in the image changes position from frame to frame.
The exact value of the Row Reset registers for this function are application dependent and the user must determine what constitutes an acceptable configuration.

10.4 Sensor Functions

10.4.1 Temperature Readout

An on-chip temperature sensor provides continuous device temperature information via the serial interface.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

Register TEMPOUT represents the actual microdisplay silicon backplane temperature and can be read at any time once the TREFDIV and TEMPOFF registers have been read from the on-board eeprom and written into the microdisplay register table using the serial interface.
To calculate the microdisplay temperature, first convert the TEMPOUT value to decimal, then use the equation below

Temperature = (TEMPOUT -69-2*dTO)/0.82

Where dTO is a calibrated value saved into the on-board eeprom at location 0x1C

The precision of the calculated value is ±2 °C
The temperature sensor is calibrated to provide a response between -50°C and +80°C

The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register PWRDN, is able to power down the sensor.

Registers TREFDIV and TEMPOFF are calibrated at the factory and their respective values are saved in the on-board eeprom at locations 16h and 17h respectively.

Figure 17 below illustrates the correlation between measured (calculated with the above formula) and actual ambient temperature for a -20°C to +60°C temperature range.

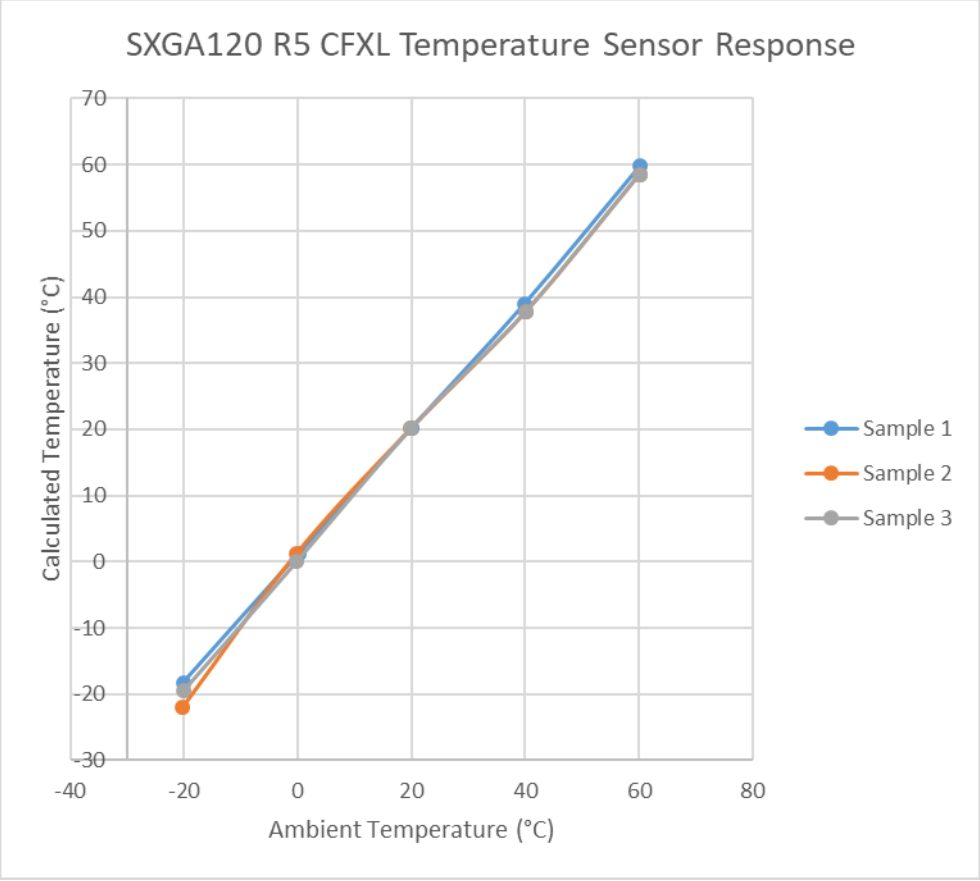


Figure 16 Temperature Sensor Response

10.4.2 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VAN supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.
The default value is 0Dh and does not have to be changed in most cases.

Register DAOFFSET[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting can be derived by measuring luminance for different values of DAOFFSET as described in 12.8.
The DAOFFSET register is calibrated at the factory and its value is saved in the on-board eeprom at location 0Ch.

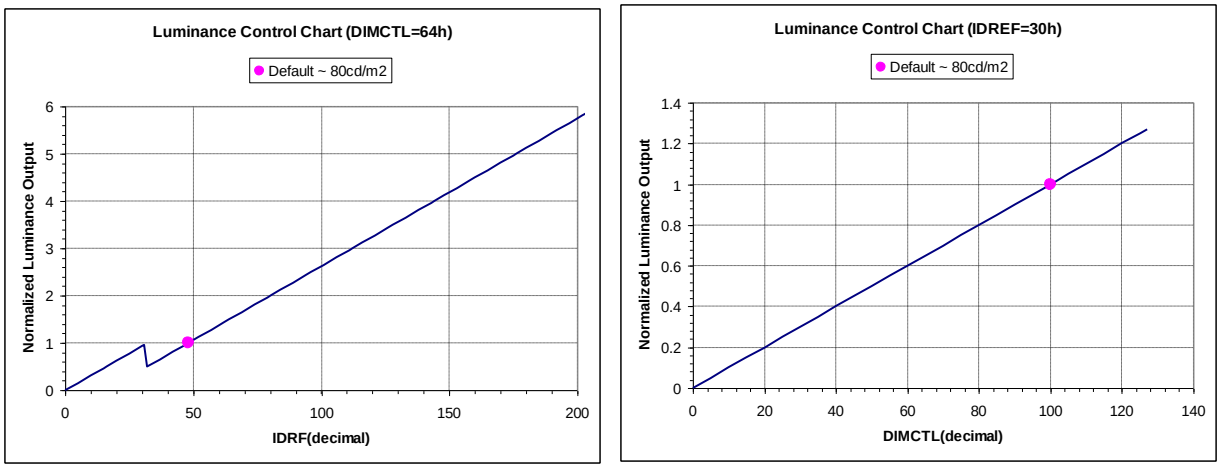
10.4.3 Pixel Bias Sensor

Register BIASN[1,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to a 10mW increase of power consumption for the array. It is recommended to use the BIASN=2 setting for best performance.

10.4.4 Luminance Control (Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. This control is also referred to as analog dimming. Dimming control for the display is effected by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRF. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRF_COARSE in register IDRF provide a coarse adjustment of the maximum luminance level, while the IDRF_FINE bits enable the coarse level to be fine-tuned. Figure 17 shows the typical luminance output at gray level = 255 in a color display for various settings of the IDRF and DIMCTL registers.



(a) (b)

Figure 17 : Typical maximum luminance for various IDRF (a) and DIMCTL (b) settings

10.4.5 Luminance Setting

The SXGA120 R5 microdisplay luminance can be set to an absolute value using information included in the on-board eeprom at addresses 5Eh to 61h.
The luminance is a linear function of IDRF for values of IDRF greater than 32 (decimal code).) that can be expressed as:

L = slope x IDRF (decimal) - intercept

The information in memory locations 5Eh (94d) to 5Fh (95d) provides the slope values that govern the Luminance vs. IDRF linear equation.
Register 5Eh provides the integer part of the slope
Register 5Fh provides the fractional part of the slope
Registers 60h & 61h provides the intercept value (Theoretical luminance value for IDRF = 0. It is theoretical because the linear equation is only valid for IDRF >20h (32 decimal)). The intercept value for the SXGA120 R5 CFXL is negative and must be subtracted from the slope x IDRF calculation.

The slope and intercept values are calibrated for each display. With these values, the calculated luminance is in cd/m^2 units (nits).

This allows precise matching between displays when used in a binocular application, as well as exceptional consistency of performance from display to display.

To calculate the luminance for IDRF values less than 20h, simply add the value 32 to the right member of the equation above

10.4.6 Luminance Control (PWM Dimming)

A variable luminance level can also be achieved by setting the frame on-time of the video image using register ROWRESET (18h). This register controls the fraction of a frame period during which the input video data is displayed (on-time). The display is set to black for the off-time or non-display portion of the frame period as shown in Figure 16.

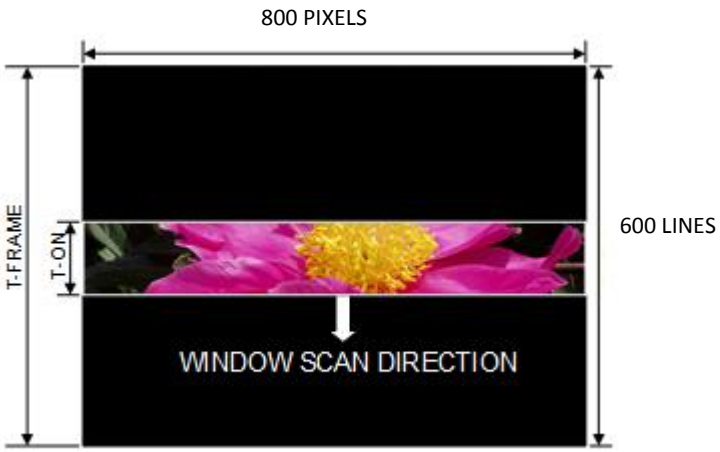


Figure 18: Video display during PWM dimming control

PWM dimming via ROWRESET can be used in combination with the analog dimming function to achieve an extended luminance control range since both modes operate independently. For any luminance level achieved via the IDRF and DIMCTL settings, the ROWRESET function will enable the luminance to be varied over a range of 0.4 to 100%.

10.4.7 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a linear optical response from the SXGA120 R5 display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The SXGA120 R5 display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value $\boldsymbol{VGN_i}$., corresponding to one of 8 internally fixed grayscale levels $\boldsymbol{GL_i}$, is selected by setting bit IDSTEP in register GAMMASET via the serial port. The VGN signal can be set for a full-scale output range of either VAN (default) or VAN/2 by setting bit VGNSEL in register GAMMASET. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear

interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN pin has a 25 Ohm nominal output impedance and can source/sink up to 200 mA

The VGN readings are normalized and converted to a 10-bit full-scale word ***DVGN$_i$[9,0]*** using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

where ***VGN$_{MAX}$*** is either VAN or VAN/2 as determined by bit VGNSEL. Each of these data values must be further multiplied by a correction factor ***CF$_i$*** to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

where the empirically determined values for factor ***CF$_i$*** are given in Table 10-1.

Table 10-1: Correction Factor values

CF0	CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.640	0.670	0.700	0.720	0.760	0.785	0.800	0.820	1

Using the derived values for ***GC$_i$*** and their corresponding grayscale coordinates ***GL$_i$***, the 8-entry Gamma Correction table consisting of data points ***Q$_i$*** = (***GL$_i$***, ***GC$_i$***) can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 10-2.

Table 10-2: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
IDSTEP[0]	0h	1h	2h	3h	4h	5h	6h	7h
VGN$_i$ (volt)	1.839	1.876	1.913	1.964	2.045	2.159	2.318	2.500

GC$_i$ (dec)	503	536	563	610	656	706	777	1023
GL$_i$ (dec)	2	4	8	16	32	64	128	255

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in Figure 19.

The input to the LUT for each color of the video source is represented by the 8-bit signal VIN[7,0], and the output of the LUT (which is also the input to the microdisplay) is represented by the 10-bit signal DIN[9,0]. For example, the Y coordinate for the intermediate point Q(x, y) on the line segment formed between the gamma table points Q6 and Q7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations. The software is also used to convert the LUT data into Gray Code format before loading it into the data-path LUTs in the FPGA. A buffer LUT should be used in the FPGA to temporarily store the data as it is transferred from the microcontroller via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

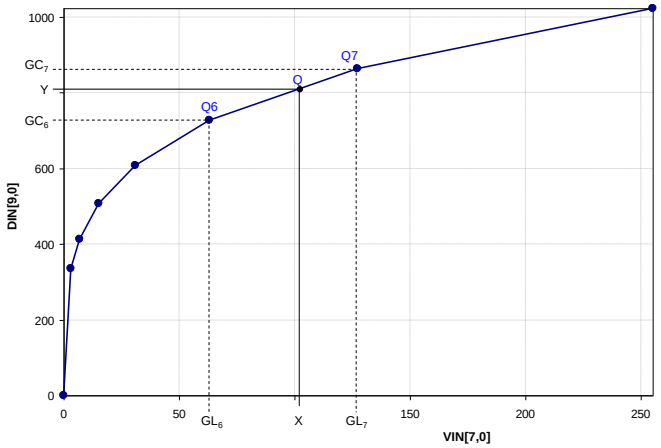


Figure 19 : Generating intermediate points by linear interpolation

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 20 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed

value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the SXGA120 R5 design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

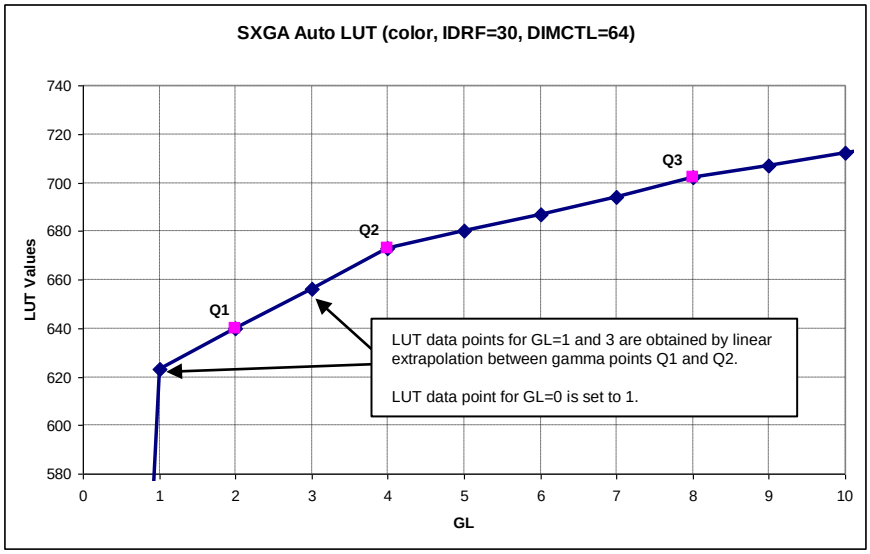


Figure 20 : Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^{\gamma}$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^{\gamma} = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^{\gamma} * 1023$$

For the case of a linear optical response (γ=1) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the System Gamma parameter are shown in Figure 21 and the corresponding system response curves for the display are given in Figure 22.

The System Gamma function is implemented in DRK Firmware V3.3 (and above) and is accessible to the user in the DRK UI Software V1.9 (and above).

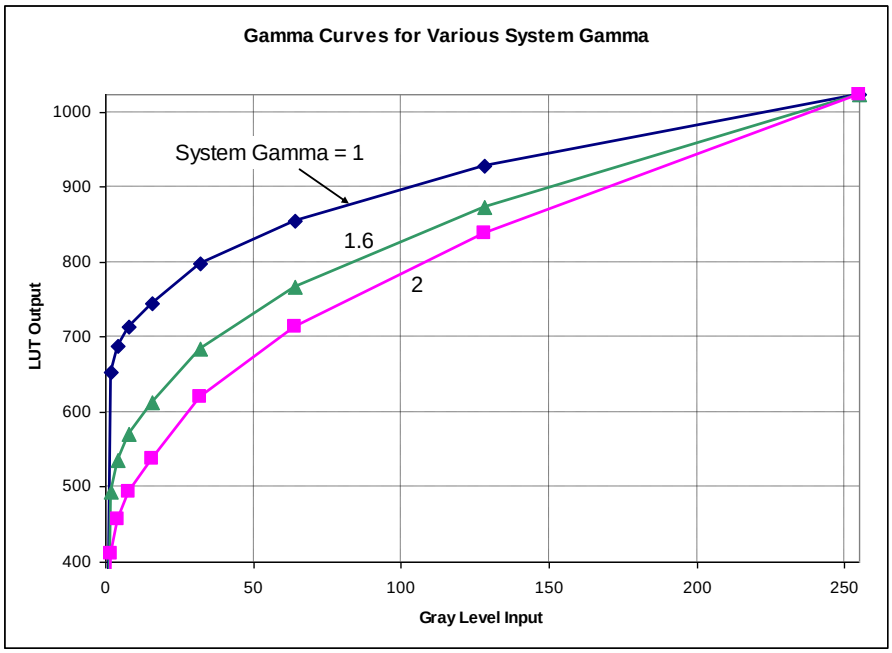


Figure 21 : Gamma curves for arbitrary System Gamma

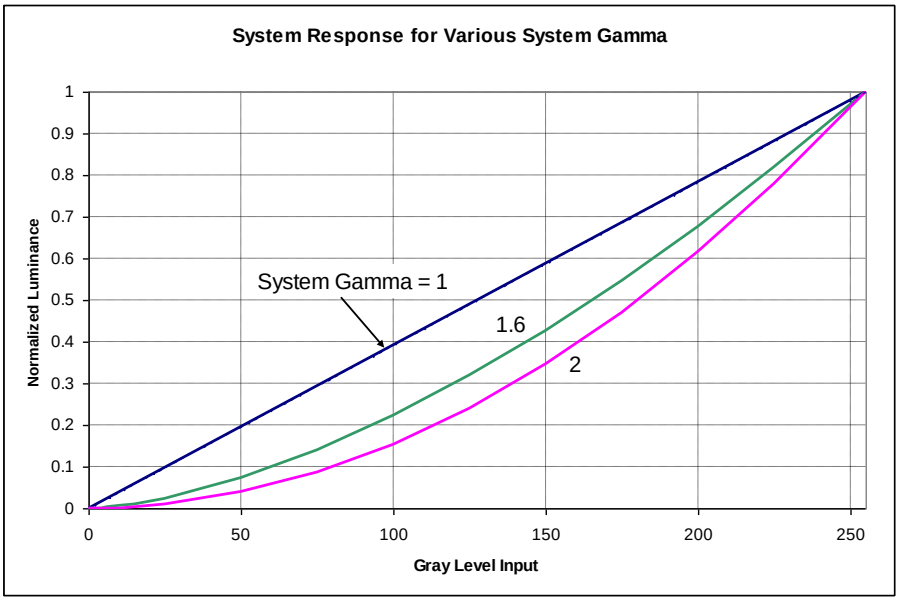


Figure 22 : Display system response for arbitrary system gamma

10.5 Fault Detection

10.5.1 Overview

The SXGA-120 R5 features internal monitoring circuits designed to detect system errors that can lead to incorrect images, be they frozen, shifted or absent.
Such detection modes are necessary for some applications and the SXGA-120 R5 provides the means to inform the host system either via register or hardware signal or both, that a malfunction in the circuit's operation has been detected.

The register signaling is built into the SXGA-120 R5 design and can be used with the standard display configuration. A dedicated register (FAULTFLAG at address 1Fh) can be polled to get information on whether any fault occurred.
Another dedicated register (FAULTCTL at address 1Eh) is used to enable/disable the fault detection functions.

The hardware signaling is implemented through a logic level output (FAULT) that is optionally connected to connector J1 pin 6.

10.5.2 Fault Conditions

Six functional faults can be detected by the SXGA-120 R5:

- Incoming image resolution check: checks if the incoming image is different from a 1280 x 1204 format
- Internal row sequencer check: checks the continuous operation of the row sequencer (works in either direction)
- Internal column sequencer check: checks the continuous operation of the column sequencer (works in either direction)
- Data Enable input check: checks the Data Enable (DE) signal is active
- Hsync input check: checks the presence of an active Hsync input
- Vsync input check: checks the presence of an active Vsync input

The detection functions can be enabled individually via the FAULTCTL register.
The detection functions, when enabled, are performed automatically.

10.5.3 Fault Reporting

The SXGA-120 R5 provides three error reporting means.

10.5.3.1 Register level reporting

Register 1Fh, FAULTFLAG is where the six detected faults, when enabled, are reported. The register is updated about every 100 ms.

10.5.3.2 User level reporting

Bit 7 of the FAULTCTL register provides the option to turn the display off when a fault is detected. This option is provided as a direct user alert.
. Should this happen, and the cause for the fault is still active, it will be necessary to reset bit 7 of register FAULTCTL to re-establish the display of data.

10.5.3.3 Hardware level reporting

A hardware FAULT output is available from the display IC but is not wired to connector J1 for standard configurations. With a simple resistor change, the FAULT output can be brought to J1-6, replacing a GND connection. This configuration can be special ordered directly from eMagin Corporation.

Care must be taken when trying to modify the standard SXGA-120 R5 assembly (EMA-101400-01) to connect the FAULT output: the eMagin Corporation SXGA Design Reference Kit has J1-6 wired to ground and connecting the FAULT output to ground may lead to damage of the output or even the entire microdisplay.

eMagin Corporation recommends users interested in making use of the FAULT hardware output to order the appropriate version of the SXGA120 R5 CFXL, part number EMA-100406-01

10.6 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0] and VCOMMODE[1,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A block level schematic of the Cuk converter that is employed in the SXGA120 R5 application is shown in Figure 23.

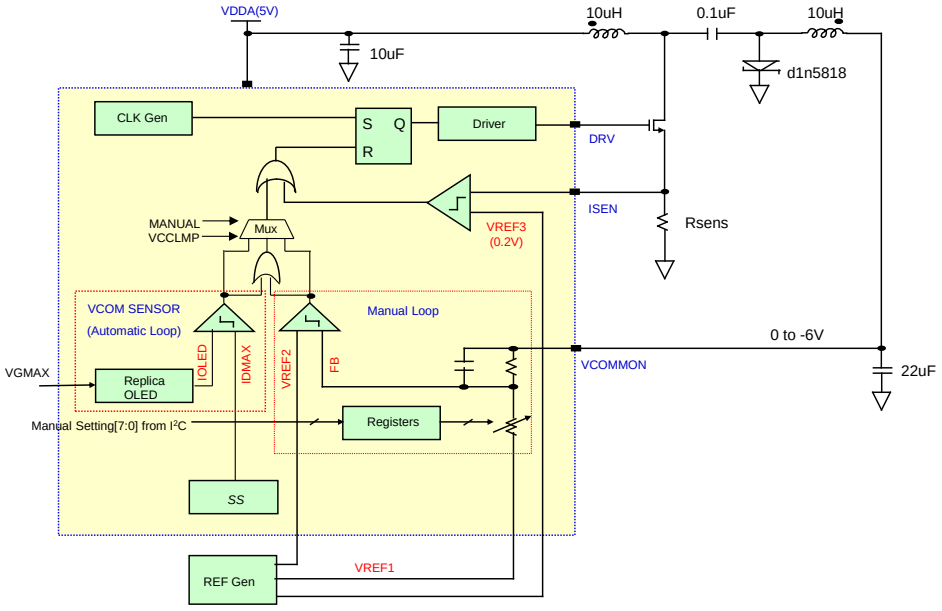


Figure 23 : Schematic of DC-DC controller function

Three modes of operation, selected via register VCOMMODE, are provided for the controller function.

Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over

changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=1h, is a hybrid control mode that prevents the absolute value of the cathode supply from becoming too small at higher temperatures, but allows it to increase at low temperatures where it is needed to ensure a stable regulated OLED current. Both the AUTO and MANUAL control loops are running simultaneously in this mode with one taking charge above a user defined threshold (set by register VCOM) and the other below that threshold. For relatively low temperatures and high luminance levels the AUTO mode will be in control and the cathode supply will follow the trajectory shown in Figure 24. If operating conditions try to force the absolute value of the cathode supply to drop below the threshold, then the control switches to MANUAL mode and the regulated supply remains fixed at the VCOM level.

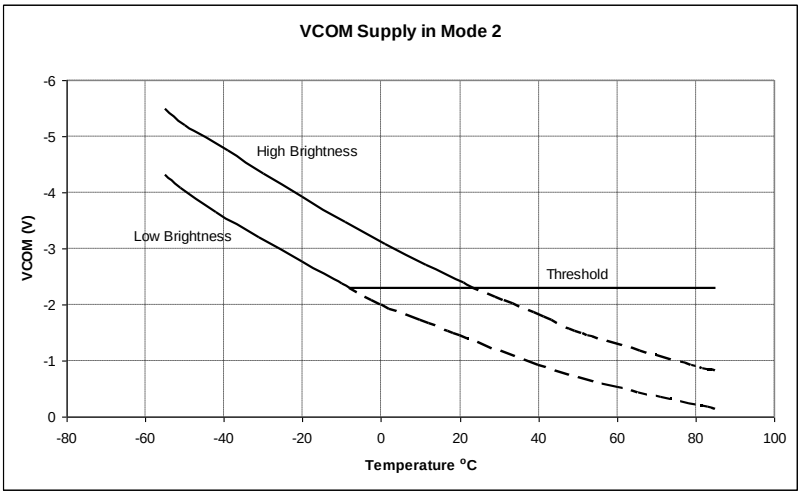


Figure 24 : VCOM supply characteristic in Mode 2

Mode 3, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the dimming and luminance regulation functions via IDRF and DIMCTL are not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.

Note: eMagin recommends using Mode 1 for typical applications.

10.7 I²C Serial Interface

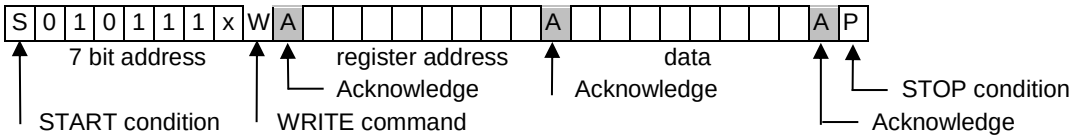
The serial interface consists of a serial controller and registers. The serial controller follows the I²C protocol. An active SCLK is required for the I²C interface to be operational. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

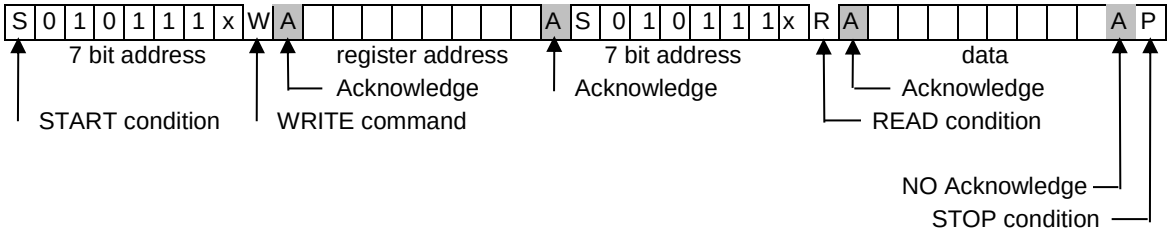
The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The serial controller is capable of slave mode only.
The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010111X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 9-3

Write Mode: Address is 5C (or 5E if SERADD = 1)

Read Mode: Address is 5D (or 5F is SERADD =1)

Sequential Read/Write Operation:
The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).
Maximum interface frequency: 400 KHz.

Table 10-3 : I^2C Address Summary

SXGA		0	1	0	1	1	1	SA	w/r	
SA = 0	write:	0	1	0	1	1	1	0	0	= 0x 5C
	read:	0	1	0	1	1	1	0	1	= 0x 5D
SA = 1	write:	0	1	0	1	1	1	1	0	= 0x 5E
	read:	0	1	0	1	1	1	1	1	= 0x 5F

Note: When the RESETB pin is active (pulled low), the SXGA chip will pull the SDA pin low.

10.8 Power-On Sequence

To ensure proper startup and stabilization of the display the power-on sequence shown in the timing diagram of Figure 25 is recommended.

Figure 25 : Power-On sequence for supplies and control.

NOTE: Do not apply VAN without a VDD supply first. This will result in high current and possible device damage!

The recommended key steps in the startup procedure are described below:

1. Turn on VDD, VAN, and VPG supplies – these can be simultaneous however the VDD supply should stabilize before the VAN supply reaches its turn-on threshold. A ramp-up time of 0.05 to 10ms for VAN and VDD is recommended for best performance, but not required. The turn-on time for VPG is not critical and it can be switched on any time before the video data to the display is enabled.
2. Initialize the display registers – writing the values of register settings for the startup state of the display should be completed next.
3. Update the gamma look-up-table (LUT) if desired, the gamma for the display can be set after step 4 is completed. Using either a preset table or the gamma update feature described in section 10.4.7, the values for the gamma look-up-table are generated and uploaded to the external FPGA driver.
4. Turn on the display – after completion of step 5 the video data to the array is enabled by setting the DISPOFF bit in register DISPMODE to “0”. Prior to enabling video data the pixels in the array are actively driven to the black state.

The currents supplied during a typical startup operation are illustrated in Figure 26. An inrush current (1) occurs on the 5V supply line during the initial moments of the ramp up phase (this is about 1A peak for a 100usec ramp time). Typically, using the startup procedure illustrated in Figure 25 the image will become active about 250 msecs after power is applied. The current drawn from the 5V supply during normal operation (2) depends on the operating luminance.

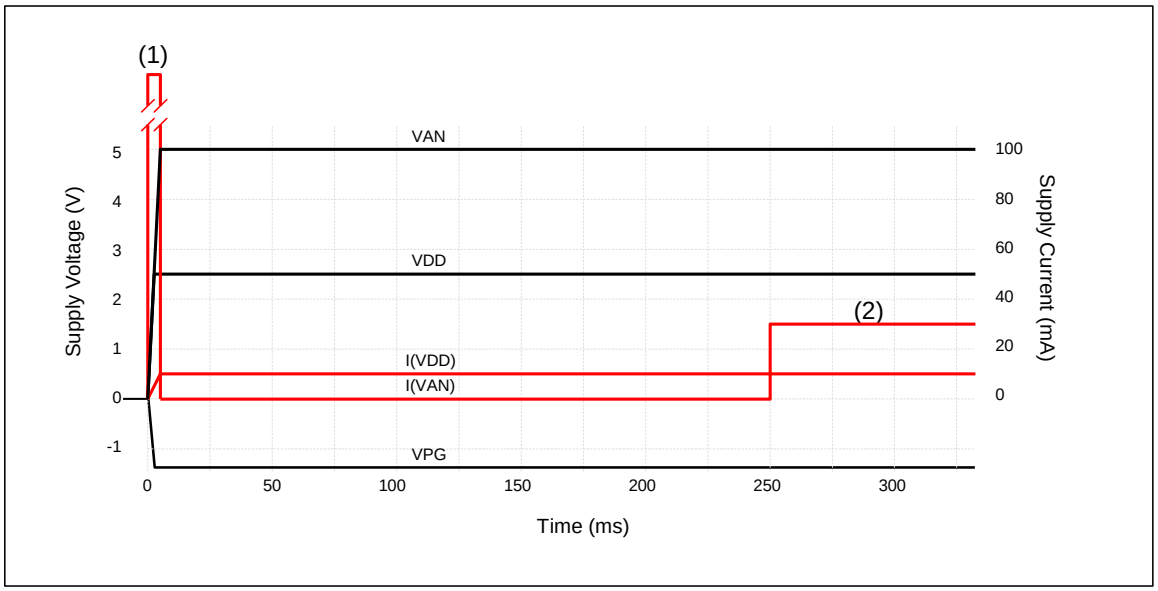


Figure 26: Typical startup currents

10.9 Power-Off Sequence

To turn the SXGA-120 R5 off, simply turn off Van first, then VDD and VPG simultaneously or with VPG immediately after turning off VDD. There is no minimum timing requirement, VDD may be turned off at the same time as VAN.

10.10 Power-Savings Mode

The display provides power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register PWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control – several functional blocks have the option to be turned off manually via control of register PWRDN.

10.10.1Display-Off Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the off state (black) until a software reset is externally applied. The DISPOFF bit in the DISPMODE register must be set to zero via the serial port in order for the array to become active.

11. REGISTER MAP SUMMARY

I2C Slave Address : 0101 11x

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STAT	R	REV	2-0	5	Silicon Revision Number
01	VINMODE	R/W	SRESET	5	0	Software Reset. Clear all registers to default setting and hold until released. 0 = Released, 1 = Software Reset
			Reserved	4	0	Not used
			SET_ENABLE	3	0	ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high
			SET_FIELD	2	0	FIELD Polarity 0 = Odd Field when ENABLE=Active, 1 = Even Field when ENABLE=Active
			VSYNCPOL	1	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			HSYNCPOL	0	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
02	DISPMODE	R/W	DISPOFF	5	1	Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off
			3D-MODE	4	0	3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode
			RESOLUTION	3	0	Display Resolution 0 = SXGA/HD720, 1=DVGA (line & pixel doubling active)
			SCMODE	2	0	Progressive or Interlaced scan mode select 0 = Progressive, 1 = Interlaced
			VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
			HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
03	TOPPOS	R/W		7-0	06	Row Display Top Position (SXGA=06h, VGA=26h, 170M=26h, 720P=9Eh)
04	BOTPOS	R/W		7-0	06	Row Display Bottom Position (SXGA=06h, VGA=26h, 170M=26h, 720P=9Eh)
05	RAMPCTL	R/W	Reserved	7-0	0	Not used
			FLYBTIME	6	0	Ramp Fly back Time 0 = 500 nSec, 1 = 800 nSec
			RAMPDLY	5-4	1	Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK
			Reserved	3-0	0	Not used
06	RAMPCM	R/W	Reserved	7-0	06	Not used
07	DAOFFSET	R/W	DAOFFSETH	7-4	0	Ramp DAC Max Value Control, Up to +20 %
			DAOFFSETL	3-0	0	Ramp DAC Max Value Control, Down to -20 %
08	EXTRAMPCTL	R/W	IRAMPHIGH	6	0	Internal Ramp DAC set All High (Active High)
			Reserved	5-0	20	Not used
09	Reserved	R/W		1-0	0	Not used
0A	BIASN	R/W	BIASN	1-0	1	00 = bias current off 01 = bias current set to 0.5nA 10 = bias current set to 1nA
0B	GAMMASET	R/W	VGNSEL	3	1	VGN Output select (Fixed to set VGN/2) 0 = Full VGN output, 1 = VGN/2 output
			IDSTEP	2-0	0	Current level for gamma sensor
0C	VCOMMODE	R/W		1-0	0	00 = AUTO1 mode 01 = AUTO2 mode 10 = MANUAL mode
Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
0D	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
0E	VCOM	R/W		7-0	51	VCOM manual setting (used when VCOMMODE = 01 or 10 , default = -2.3V)
0F	IDRF	R/W	IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
			IDRF_FINE	4-0	0	Fine adjustment for array reference current
10	DIMCTL	R/W		6-0	01	Dimming level control (default = 1X IDRF)
11	TREFDIV	R/W		5-0	17	Temp. Sensor Reference Clock Divider
12	TEMPOFF	R/W		7-0	3A	Temp. Sensor Offset
13	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * $PERIOD_{FRAME}$ $PERIOD_{FRAME}$ = 16.6 mSec when using 60Hz Video
14	TEMPOUT	RO		7-0	-	Temperature Sensor Readout

12. DETAILED REGISTER DESCRIPTIONS

12.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
REV	2-0	5	Silicon revision number; 5 is for R5

This register indicates the revision number of the silicon backplane design.

12.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SRESET	5	0	Software reset
Reserved	4	0	Not used
SET_ENABLE	3	0	ENABLE active level
SET_FIELD	2	0	Field polarity
VSYNCPOL	1	1	VSYNC polarity
HYSYNCPOL	0	1	HSYNC polarity

SRESET:

1 = all internal registers are reinitialized to their default values and held there
0 = releases all internal registers from default state so they can be updated externally via I^2C (default)

SET_ENABLE:

0 = the active state of the ENABLE input is set “low” (default)
1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single

video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

The ENABLE input pin is also used to indicate field polarity in non-3D interlaced modes. In this mode the SET_FIELD bit determines the field polarity when ENABLE is active.

SET_FIELD:

0 = Odd Field when ENABLE=Active (default)
1 = Even Field when ENABLE=Active

The SET_FIELD register determines the field polarity of the video signal when the ENABLE pin is active.

VSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

HSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

12.3 DISPMODE (02h)

Name	DISPMODE
Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description

DISPOFF	5	1	Display On/Off control
3D-MODE	4	0	3D Mode control
RESOLUTION	3	0	Display resolution selection
SCMODE	2	0	Progressive or Interlaced scan mode selection
VSCAN	1	0	Vertical Scan direction
HSCAN	0	0	Horizontal Scan direction

DISPOFF:

0 = Display is turned ON
1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

3D-MODE:

0 = Normal display mode (default)
1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE=”1” the SCMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h). The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= “0”, bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE=”1”, bit #3 of the VINMODE register). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

RESOLUTION:

0 = SXGA / HD720 resolution (default) and all other non-DVGA custom modes
1 = DVGA resolution (line and pixel doubling active)

SCMODE:

0 = Progressive scan mode (default)
1 = Interlaced scan mode

Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field.

VSCAN:

0 = Top to Bottom vertical scan direction (default)
1 = Bottom to Top vertical scan direction

HSCAN:

0 = Left to Right horizontal scan direction (default)
1 = Right to Left horizontal scan direction

12.4 TOPPOS (03h)

Name	TOPPOS
Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Top position of first active row

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can be moved by ±6 lines from the center (default) position. Decreasing TOPPOS will shift the active window upwards in the display window. When TOPPOS is decreased, register BOTPOS must be increased by the same value so that the sum of the two remains equal. See BOTPOS for some typical settings.

12.5 BOTPOS (04h)

Name	BOTPOS
Address	04h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Bottom position of last active row

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can

be moved by ±6 lines from the center (default) position. In HD720 mode the active window can be moved by a maximum of ±255 lines from the center position. In DVGA mode the active window can be moved by ±38 lines from the center position. Increasing BOTPOS will shift the active window upwards in the display window. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal. Typical settings are given in the following table:

Vertical Position	Register	SXGA	DVGA	720P
Top	TOPPOS	00	00	3D
	BOTPOS	0C	4C	FF
Center	TOPPOS	06	26	9E
	BOTPOS	06	26	9E
Bottom	TOPPOS	0C	4C	FF
	BOTPOS	00	00	3D

12.6 RAMPCTL (05h)

Name	Reserved
Address	05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7-0	10	Reserved – Do not change

12.7 RAMPCM (06h)

Name	Reserved
Address	06h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7-0	44	Reserved – Do not change

12.8 DAOFFSET (07h)

Name	DAOFFSET
Address	07h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DAOFFSETH	7-4	0	RAMP DAC maximum value increase control
DAOFFSETL	3-0	0	RAMP DAC maximum value decrease control

DAOFFSETH:

0h = no change (default)
Fh = +20% change

DAOFFSETL:

0h = no change (default)
Fh = -20% change

Registers DAOFFSETH and DAOFFSETL are used to adjust the maximum value of the internal RAMP DAC signal. DAOFFSETH can increase the maximum level by up to +20% and DAOFFSETL can decrease the maximum level by up to -20% of the nominal value.

The typical dependence of display luminance on DAOFFSET(d) is shown in Figure 27. The luminance is seen to saturate for DAOFFSET greater than 4 in this sample. For normal operation DAOFFSET should be set to about 88% of the saturation value as shown in the figure.

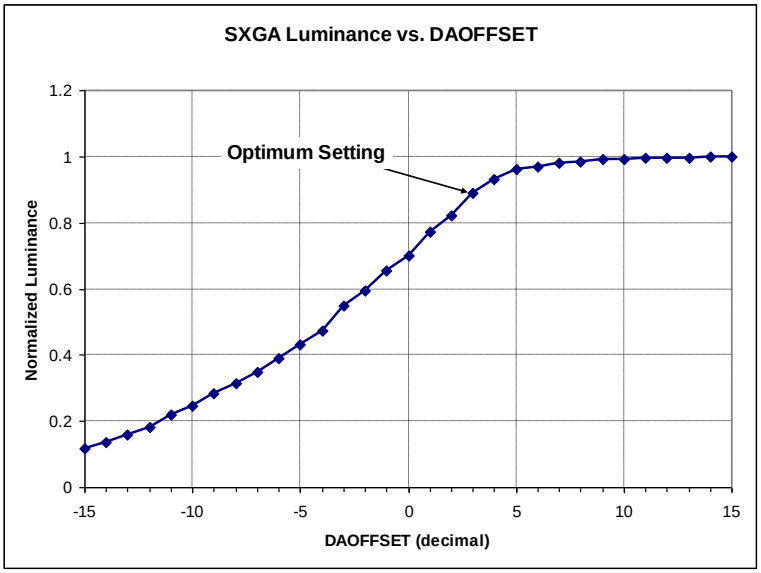


Figure 27: Luminance dependency on DAOFFSET

12.9 EXTRAMPCTL (08h)

Name	Reserved
Address	08h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7-0	20	Reserved – Do not change

12.10 Reserved (09h)

Name	Reserved
Address	09h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	1-0	0	Reserved – Do not change

12.11 BIASN (0Ah)

Name	BIASN
Address	0Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	1	Set pixel bias current

BIASN:

00 = pixel bias current is turned off
01 = pixel bias current set to 0.5nA (default)
10 = pixel bias current set to 1nA

The BIASN register is used to set the sink current applied in each pixel cell.
It is recommended to use the BIASN=10 setting in normal operation for best performance.

12.12 GAMMASET (0Bh)

Name	GAMMASET

Address	0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
VGNSEL	3	1	VGN output range setting
IDSTEP	2-0	0	Current level for gamma sensor

VGNSEL:

0 = Full VGN output range, 0 to VAN
1 = VGN/2 output range, 0 to VAN/2 (default)

The VGNSEL register is used to select the VGN signal output range. It can be set to either 0 to VAN or 0 to VAN/2.

IDSTEP:

0h ≈ IDRF/128
1h ≈ IDRF/64
2h ≈ IDRF/32
3h ≈ IDRF/16
4h ≈ IDRF/8
5h ≈ IDRF/4
6h ≈ IDRF/2
7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

12.13 VCOMMODE (0Ch)

Name	VCOMMODE
Address	0Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	0	Set internal VCOM supply mode

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
01 = AUTO2 mode
10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.
In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.
In the Auto 3 mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

eMagin Corporation recommends setting VCOMMODE to Mode 1 (00h) for normal operation.

12.14 VGMAX (0Dh)

Name	VGMAX
Address	0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

00h = 5 (VAN = 5V)
0Dh = 4.95 (default)
FFh = 4

VGMAX level = VAN*(1 - 0.2*VGMAX(dec) / 255)

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VAN supply to prevent saturation of the video buffer amplifiers.

12.15 VCOM (0Eh)

Name	VCOM
Address	0Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	**51***	40	30
Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	**-2.4**	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE =01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply ≈ -2.3V. The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 28 for a color display.

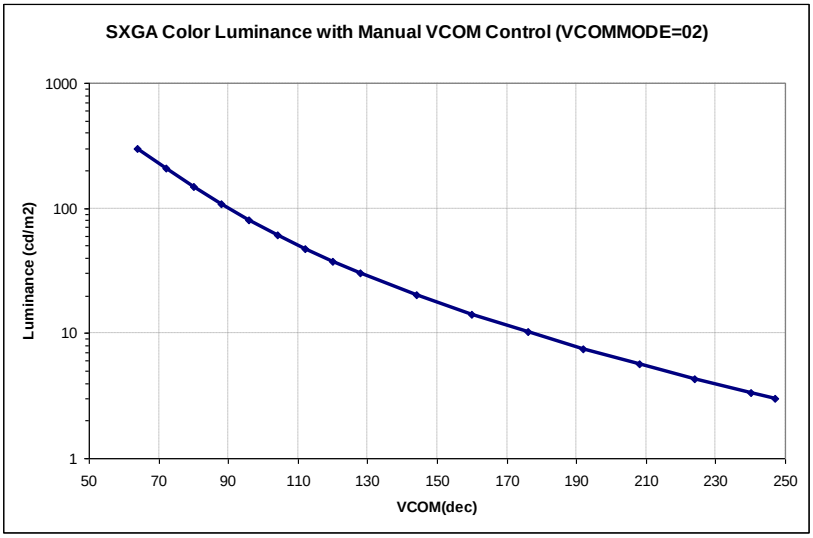


Figure 28: Typical luminance dependency on manual VCOM setting

12.16 IDRF (0Fh)

Name	IDRF
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
IDRF_FINE	4-0	00	Fine adjustment for array reference current

IDRF_COARSE (IC):

IC#
0h = 0 (default)
1h = 0.5
2h = 1.5
3h = 2.5
4h = 3.5
5h = 4.5
6h = 5.5
7h = 6.5

IDRF_FINE (IF):

IF#
00h = 0 (default)
01h = 1/32
…
10h = 16/32
…
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF as given by the following expression:

LMAX = LDEF*(IC# + IF#) in cd/m^2
Where LDEF is the luminance for IDRF = 0x30

This register is only operational in Auto VCOM mode (VCOMMODE=00).
Note that the SXGA120 R5 implementation limits the maximum IDRF hex value to 0xD8. Values greater than 0xD8 will not continue to increase luminance.

Also note that the same luminance will be reached for IDRF = 0x10 to 0x1E and IDRF = 0x20 to 0x2E. This is how the control logic was implemented.

Error! Reference source not found. shows the relation between IDRF (hex values) and the IC# and IF# values

Table 4: IDRF vs. IC# + IF#

IDRF (hex)	IC# + IF#
0	0
10	0.5
20	0.5
30	1
40	1.5
50	2
60	2.5
70	3
80	3.5
90	4
A0	4.5
B0	5
C0	5.5
D0	6

12.17 DIMCTL (10h)

Name	DIMCTL
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	01	Dimming level control

00h = 0
01h = 1% of LMAX
…
64h = 100% of LMAX
…
7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 64h is equal to 100% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

12.18 TREFDIV (11h)

Name	TREFDIV
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	17	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -46 to 80^{o}C, although the setting is best determined by a calibration measurement of the display in its final assembly.

The recommended default value for TREFDIV is 0x14 and must be read from the eeprom (location 0x16) and written to this register whenever the SXGA120 R5 CFXL

See the description for register TEMPOUT.

12.19 TEMPOFF (12h)

Name	TEMPOFF
Address	12h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	3A	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

The recommended default value for TEMPOFF must be read from the eeprom (location 0x17) and written to this register whenever the SXGA120 R5 CFXL microdisplay is powered on

See the description for register TEMPOUT.

12.20 TUPDATE (13h)

Name	TUPDATE
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

$$\text{Update Time} = (\text{TUPDATE(decimal)} + 1) * T_{FRAME}$$

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

12.21 TEMPOUT (14h)

Name	TEMPOUT
Address	14h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The SXGA display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (13H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user.

Temperature = (TEMPOUT -69- 2*dTO)/0.82

Where dTO is a calibration value saved into the on-board eeprom at location 0x1C

eMagin Corporation calibrates each microdisplay temperature sensor as part of its manufacturing process. The temperature is done at room ambient (~ 20°C) and the values of TREFDIV and TEMPOFF are recorded in the on-board EEPROM at locations 16h and 17h respectively.

If, for some reason, it becomes necessary to recalibrate the temperature sensor (determine the optimum values of the TEMPOFF register), the following procedure can be used:

To get a reasonably good sensor performance it is usually enough to just find the optimum value for TEMPOFF which requires only one measurement at room temperature.

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV = 0x14 (20 decimal)
- Set TEMPOFF = 0xAD (173 decimal)
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read $TEMPOUT_{AMB}$ and the ambient temperature T_{AMB}

- The optimum value for TEMPOFF is then given by

  TEMPOFF = TMPOUT =88

This value of TEMPOFF is the one that should then be written into the eeprom at address 0x17

dTO is calculated by the following equation: dTO = TEMPOUT – 85

This value of dTO is the one that should be written into the eeprom at address 0x1C

12.22 PWRDWN (15h)

Name	PWRDWN
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PDWN	7	0	All systems power down
RDACPD	6	0	RAMP DAC power down
BIASGENPD	5	0	BIASGEN power down
TRAMPPD	4	0	Top RAMP buffer amp power down
BRAMPPD	3	0	Bottom RAMP buffer amp power down
VCMBP	2	0	VCOM generator bypass and power down
TSENDP	1	0	Temperature sensor power down
Reserved	0	0	Not used

PDWN:

1 = all systems are powered down
0 = normal operation (default)

By setting the PDWN bit to a "1" the chip enters a deep sleep mode in which all functions including the I^2C interface are powered down in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I^2C input lines and resets the PDWN bit when it detects the correct I^2C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

RDACPD:

1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

BIASGENPD:

1 = Bias generator is powered down
0 = Bias generator is operating normally (default)

When set to 1, the display image will dim and a bright flash will occur every half second or so. eMagin Corporation recommends to keep this bit set to 0 at all times.

TRAMPPD:

1 = the top RAMP buffer amplifier is powered down
0 = the top RAMP buffer is operating normally (default)

When set to 1, the display will not output any image (blank screen). The register interface remains active

BRAMPPD:

1 = the bottom RAMP buffer amplifier is powered down
0 = the bottom RAMP buffer is operating normally (default)

When set to 1, the display will not output any image (blank screen). The register interface remains active

VCMBP:

1 = the dc-dc converter used to generate VCOM is bypassed and powered down
0 = the dc-dc converter is operating normally (default)

The internal VCOM generator may be deactivated if an external VCOM supply is used.

When set to 1, the display image will remain at a constant brightness and will respond to any change in either IDRF, DIMCTL or VCOM registers.

TSENDP:

1 = the Temperature Sensor is powered down
0 = the Temperature Sensor is operating normally (default)

The temperature sensor can be turned off by register TSENDP when a temperature readout is not needed.

12.23 TPMODE (16h)

Name	TPMODE
Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	2-0	0	Select test pattern for Burn-In mode

The BI pin must be tied high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)
001 = color bar pattern
010 = gray scale pattern without gamma correction
011 = checkerboard pattern
100 = alternating columns pattern
101 = alternating rows pattern
110 = alternating columns and rows pattern
111 = gray level pattern (007h gray color)

12.24 Reserved (17h)

Name	Reserved
Address	17h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved – Do not change

12.25 ROWRESET (18h, 19h)

Name	ROWRESET
Address	18h, 19h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ROWRESETL (18h)	7-0	0	Row duty rate control (LSB)
ROWRESETH (19h)	1-0	0	Row duty rate control (MSB)
	4	0	ROWRESET work on UNENABLED frame in 3D mode

ROWRESETH:BIT4

0 = Active duty rate can be set 0 ~ 50%, 100% when 3D mode
1 = Active duty rate can be set 50 ~ 100% when 3D mode

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

ROWRESET (dec)	Active Line Cycles	Active Duty Rate (%)	Note
0	all	100	Pixels active for entire frame period
1	2	$2*T_{HSYNC}/T_{FRAME}$	1054 total HS cycles / frame (SXGA/60Hz)
n	2*n	$2*n*T_{HSYNC}/T_{FRAME}$	

Figure 29 below shows the display luminance as a function of the ROWRESET register value

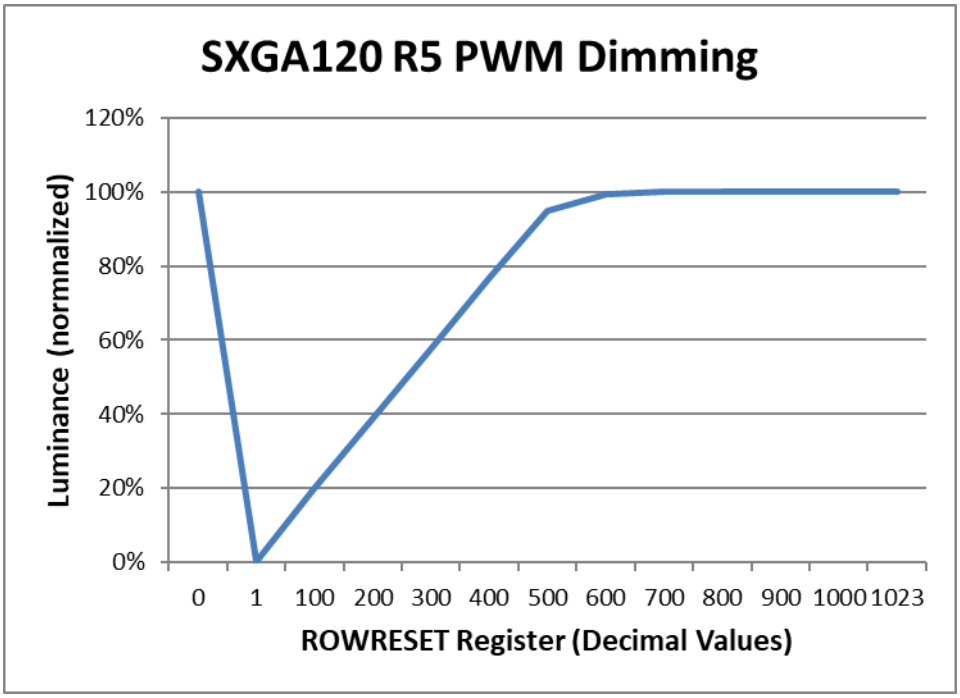


Figure 29 SXGA120 Luminance vs. ROWRESET

12.26 VCOMCTL (1Ah)

Name	VCOMCTL
Address	1Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7	0	Do not change
Reserved	6-4	3	Do not change
VCKSEL	3-2	3	VCOM clock select
VCOMSS	1-0	1	VCOM soft start delay time

The reserved locations must be kept as per the reset value.
VCKSEL:
The VCKEL bits select one of 3 possible operating frequency for the VCOM dc-dc converter. Maximum efficiency is achieved with the default setting.

0h = Reserved, do not use.
1h = 250 kHz
2h = 500 kHz
3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.

VCOMSS:

0h = 2 ms
1h = 4 ms (default)
2h = 8 ms
3h = 16 ms

Register VCMOSS sets the soft-start duration during startup of the VCOM converter.

12.27 NVCK0 (1Bh)

Name	NVCK0
Address	1Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7-0	99	Reserved – Do not change

12.28 NVCK1 (1Ch)

Name	NVCK1
Address	1Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	7-0	99	Reserved – Do not change

12.29 LDO_CTL (1Dh)

Name	LDO_CTL
Address	1Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	2-0	3	Reserved – Do not change

12.30 FAULTCTL (1Eh)

Name	FAULTCTL
Address	1Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
FLTDISPOFF	7	0	Enable Display off when FAULT detected
RESDEN	6	0	Input video resolution check enable
ROWDEN	5	0	Row sequencer fault check enable
COLDEN	4	0	Column sequencer fault check enable
DEDEN	3	0	DATAEN fault check enable
HSDEN	2	0	HSYNC fault check enable
VSDEN	1	0	VSYNC fault check enable
CLKDEN	0	0	SCLK fault check enable

Fault detection function enables when any of FAULTCTL bit from CLKDEN(bit0) to RESDEN(bit6) is set to “1”. And none of FAULTCTL[6:0] is enabled (all “0”) then the internal fault detection circuit is shut down.
When FAULT signal is detected, the related FAULTFLAG register bit will be set to “1” and FAULT signal pin goes to active(high). . When FAULTDISPOFF bit is set to “1” ,the display is automatically OFF if one of FAULT is detected.

FLTDISOFF:
0 = Disable display off when FAULT function
1 = Enable display off when FAULT function

RESDEN: Check video resolution every 6th Frames. Input video resolution is compared with resolution of 1292X1024.
0 = Disable input video resolution check function
1 = Enable input video resolution check function

ROWDEN: Check row sequencer last shift register out and it should be detected more than 3 times within 0.1 seconds. Front pouch of input video blanking period should be more than "1036 - <number of active video lines>" otherwise row fault check may FAULT always.
0 = Disable row sequencer fault check function
1 = Enable row sequencer fault check function

COLDEN: Check column sequencer last shift register out and it should be detected more than 8 times within 0.1 seconds.
0 = Disable column sequencer fault check function
1 = Enable column sequencer fault check function

DEDEN: DATAEN signal should be detected more than 8 times within 0.1 seconds.
0 = Disable DATAEN fault check function
1 = Enable DATAEN fault check function

HSDEN: HSYNC signal should be detected more than 8 times within 0.1 seconds and HSYNC signal should detected between DATAEN signals.
0 = Disable HSYNC fault check function
1 = Enable HSYNC fault check function

VSDEN: VSYNC signal should be detected more than 3 times within 0.1 seconds and VSYNC signal should be detected before DATAEN appears after 2 or more blanking lines.
0 = Disable VSYNC fault check function
1 = Enable VSYNC fault check function

CLKDEN: The system clock (SCLK) should be detected more than 8 times within 0.1 seconds.
0 = Disable SCLK fault check function
1 = Enable SCLK fault check function

12.31 FAULTFLAG (1Fh)

Name	FAULTFLAG
Address	1Fh
Mode	Read / Clear

Bit Name	Bit#	Reset Value	Description
RESFLT	6	-	Input video resolution check fail
ROWFLT	5	-	Row sequencer fault
COLFLT	4	-	Column sequencer fault
DEFLT	3	-	DATAEN fault (No DATAEN input)
HSFLT	2	-	HSYNC fault (No HSYNC input)
VSFLT	1	-	VSYNC fault (No VSYNC input)
CLKFLT	0	-	SCLK fault (No SCLK input)

The FAULTFLAG registers indicate which fault is detected. Once a FAULT is detected, the FAULTFLAG register will be set to high and stay in active even the fault condition is disappeared as long as it is not cleared by I2C operation. To clear the FAULTFLAG register, we have to write any data to the FAULTFLAG register. The clear operation is applied to all of the flag registers at the same time. It cannot be applied to each flag individually.
All FAULTFLAG bits are updated every 0.1 second period. Each flag bits can be masked by FAULTCTL bit 0 to 6.

RESFLT:
0 = Input video resolution is 1292X1024
1 = Input video resolution is not 1292X1024

ROWFLT:
0 = Row sequencer works well
1 = Row sequencer fault detected
- When VSCAN=0, bottom most row driver output check
- When VSCAN=1, top most row driver output check

COLFLT:
0 = Column sequencer works well
1 = Column sequencer fault detected
- When HSCAN=0, right most top/bottom column sequencer output check
- When HSCAN=1, left most top/bottom column sequencer output check

DEFLT:
0 = DATAEN input signal provided
1 = No DATAEN input signal is detected

HSFLT:
0 = HSYNC input signal provided
1 = HSYNC input signal fault is detected
- No HSYNC signal detected within 0.1 seconds detection period
- No HSYNC signal detected between DATAEN signals

VSFLT:
0 = VSYNC input signal provided
1 = VSYNC input signal fault is detected
- No VSYNC signal detected within 0.1 seconds detection period
- No VSYNC signal detected between Active Video (group of DATAEN & HSYNC) signals[*1]

CLKFLT:
0 = SCLK input provided
1 = No SCLK input signal is detected

12.32 NOFPIXEL (20h, 21h)

Name	NOFPIXEL
Address	20h, 21h
Mode	Read only

Bit Name	Bit#	Reset Value	Description
NOFPIXELL (20h)	7-0	-	Number of active pixel per line (LSB)
NOFPIXELH (21h)	10-8	-	Number of active pixel per line (MSB)

Count number of active pixel per line every 64th Frames (about 1 second period in 60Hz video) and updated.

12.33 NOFLINE (22h, 23h)

Name	NOFLINE
Address	22h, 23h
Mode	Read only

Bit Name	Bit#	Reset Value	Description
NOFLINEL (22h)	7-0	-	Number of active line per frame (LSB)
NOFLINEH (23h)	10-8	-	Number of active line per frame (MSB)

Count number of active lines per frame every 64th Frames (about 1 second period in 60Hz video) and updated.

12.34 Reserved (24h – 2Ah)

Name	Reserved
Address	24h – 2Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved – Do not change

12.35 Reserved (2Bh – 2Dh)

Name	Reserved
Address	2Bh – 2Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved – Do not change

12.36 Reserved (2Eh)

Name	reserved
Address	2Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Reserved (Do not Change)

12.37 Reserved (2Fh)

Name	reserved
Address	2Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	00	Reserved (Do not Change)

APPENDIX A: APPLICATION SYSTEM DIAGRAM

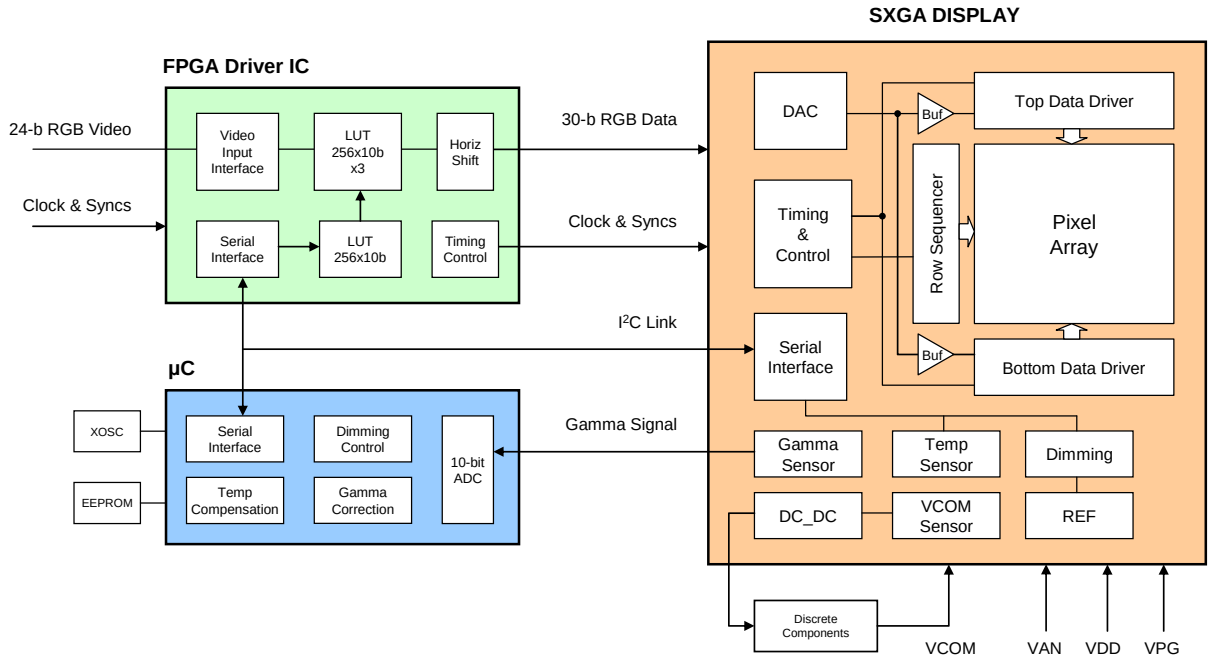


Figure 30 : Block diagram of application reference system

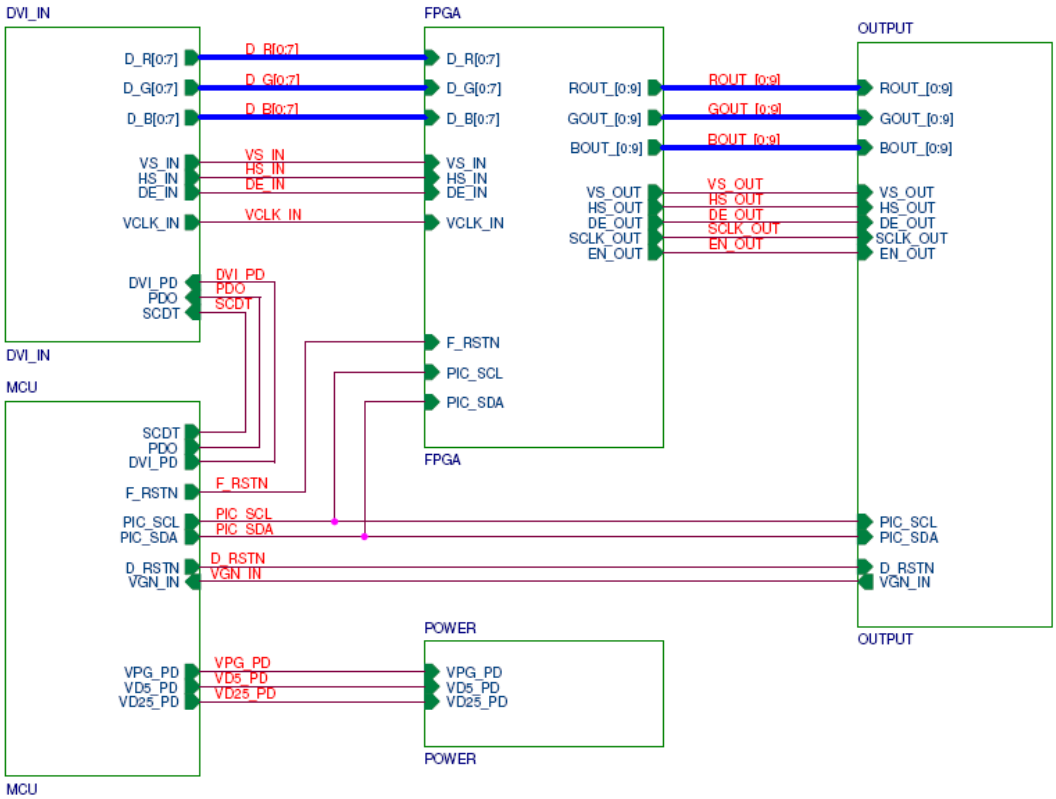


Figure 31 : Top-level schematic of development board (A01-500467-02)

13. APPENDIX B: MICRODISPLAY CARRIER BOARD

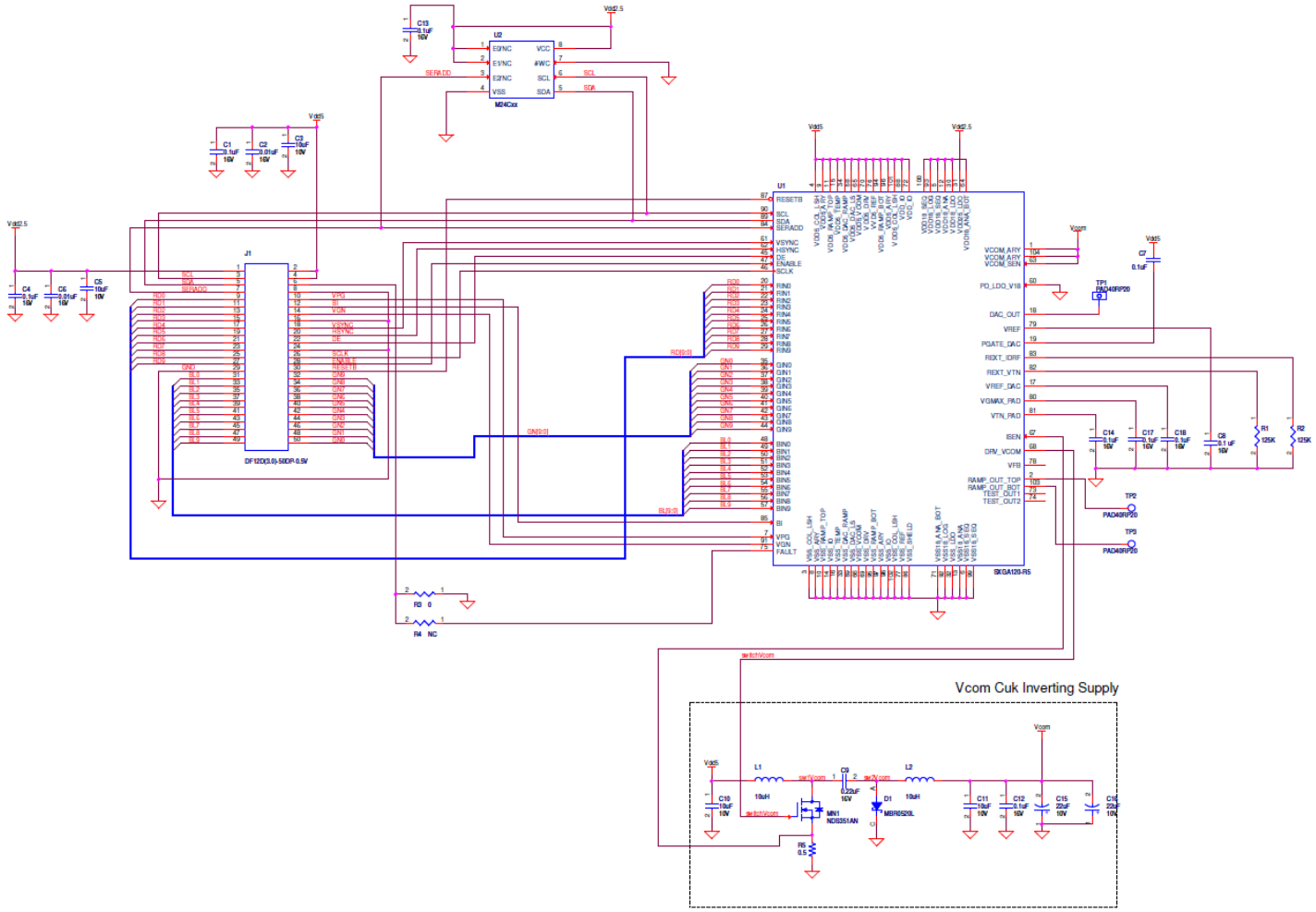


Figure 32 : Carrier board schematic (D01-501455-00)

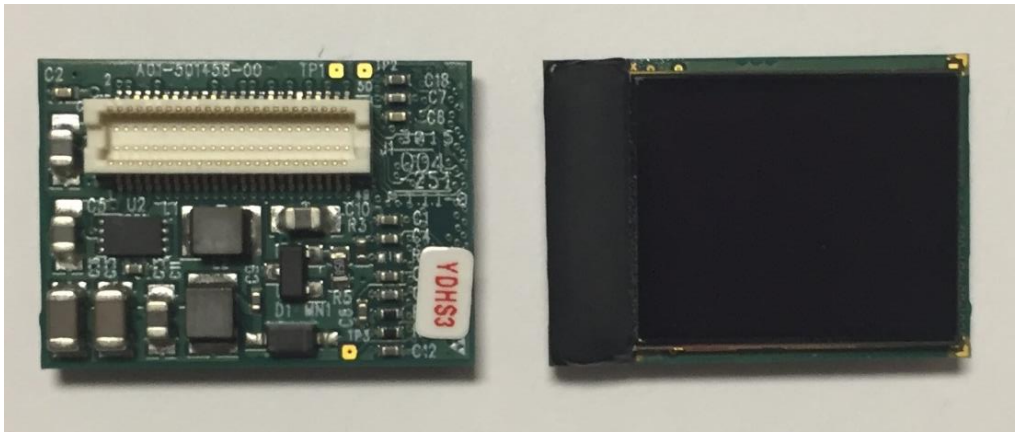


Figure 33: Photo of Microdisplay Assembly (A01-501458-00)

14. APPENDIX C: MICRODISPLAY ASSEMBLY BILL OF MATERIALS

Item #	Quantity	Reference	Description	Value	Mfg	Mfg Part #	RoHS Compliant
1	10	C1,C4,C7,C8,C12, C13,C14,C17,C18	CAP,0.1uF,16V,10%,CER,X5R, 0402	0.1uF	Murata	GRM155R61C104KA88D	Y
2	2	C2,C6	CAP CER 0.01UF 16V 10% X7R 0402	0.01uF	Murata	GRM155R71C103KA01D	Y
3	1	C9	CAP,0.22uF,16V,10%,CER,X5 R,0402	.22uF	Taiyo Yuden	EMK105BJ224KV-F	Y
4	2	C15,C16	CAP CER 22UF 10V CER X5R 1206	22uF	Taiyo Yuden	LMK316BJ226ML-T	Y
5	4	C3,C5,C10,C11	CAP CER 10UF 10V 20% X5R 0603	10uF	TDK	C1608X5R1A106M	Y
6	1	C11	CAP CER 10000pF 16V 10% X7R 0402	0.01uF	Murata	GRM155R71C103KA01D	Y
7	1	D1	DIODE SCHOTTKY 20V 0.5A SOD123	MBR0520L	Fairchild Semiconductor	MBR0520L	Y
8	1	J1	CONN HEADER 50POS 3MM SMD 0.5MM	DF12(3.0)-50DP-0.5V	Hirose Electric	DF12D(3.0)-50DP-0.5V	Y
9	2	L1,L2	INDUCTOR POWER 10UH 700MA 1210	LQH32PN100MN0L/10uH	Murata	LQH32PN100MN0L	Y
10	1	Q1	MOSFET N-CH 30V 1.4A SSOT3	NDS351AN	Fairchild Semiconductor	NDS351AN	Y
11	1	R3	RES 0.0 OHM 1/10W 0603 SMD	0	Panasonic	ERJ-3GEY0R00V	Y
12	2	R1,R2	RES 124K OHM 1/16W 1% 0402 SMD	125K(124K FOR 0402 FOOTPRINT)	Bourns Inc	CR0402-FX-1243GLF	Y
13	1	R5	RES 0.5 OHM 1/10W 1% 0603 SMD	0.5/603	YAGEO	RL0603FR-070R5L	Y
14	1	U2	EEPROM Serial-I2C 2K-Bit 256 x 8 1.8V/2.5V/3.3V/5V	NA	On Semi	CAT34C02HU4I-GT4A	Y
15	1	PCB1	PCB	C01-501457-00	Mettrix		Y

15. APPENDIX D: TYPICAL REGISTER SETTING

Address (Hex)	Name	Recommended value (Hex)	Note
00	STAT	Read-only	Read value is 05
01	VINMODE	03	
02	DISPMODE	00	
03	TOPPOS	06	
04	BOTPOS	06	
05	RAMPCTL	10	
06	RAMPCM	44	
07	DAOFFSET	50	Use EEPROM value
08	EXTRAMPCTL	20	
09	RESERVED	00	
0A	BIASN	02	
0B	GAMMASET	0F	
0C	VCOMMODE	00	
0D	VGMAX	0D	
0E	VCOM	00	
0F	IDRF		User Defined
10	DIMCTL		User Defined
11	TREFDIV	19	
12	TEMPOFF	1A	
13	TUPDATE	10	
14	TEMPOUT	Read-only	
15	PWRDN	00	
16	TPMODE	00	
17	RESERVED	44	
18	ROWRESETL	00	No PWM
19	ROWRESETH	00	No PWM
1A	VCOMCTL	3D	
1B	NVCK0	99	
1C	NVCK1	99	
1D	LDO_CTL	03	
1E	FAULTCTL	00	FAULT mode disabled
1F	FAULTFLAG	Read-only	
20	NOFPIXEL_L	0A	1292 pixels per line
21	NOFPIXEL_H	05	
22	NOFLINE_L	00	1024 active lines
23	NOFLINE_H	04	
24-2A	RESERVED	00	
2B	RESERVED	00	
2C	RESERVED	00	
2D	RESERVED	00	
2E	RESERVED	FF	
2F	RESERVED	00	

Recommended Register Settings for Normal Operation

Notes:
1. Value of register DAoffset is specific to each individual device and should be calibrated
2. Registers TrefDiv and TempOff can be adjusted for best temperature reading accuracy

16. APPENDIX E: EEPROM MEMORY MAP

The SXGA microdisplays contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation.

eMagin Corporation recommends users implement a circuit to read the EEPROM values every time the display is turned on, and use the display specific values highlighted in gray below to configure the display register for optimal operation (locations 0Ch to 17h).
The IDRF value in the EEPROM is the one that will set the display luminance to 150 ± 5 cd/m2

The data can be accessed via the same I^2C serial interface that is used to communicate with the microdisplay. The device's serial address is as follows:

Write Mode: Address is A6h (or AEh if SERADD = 1), or 0xAE (SELAD0 = 1) – ***Prohibited mode***

Read Mode: Address is A7h (or AFh if SERADD =1) , or 0xAF (SELAD0 = 1)

The first 5 bytes represent unique serial number of the SXGA microdisplay. The next 24 bytes contain sequential data values that can be used to write to the microdisplay's internal registers starting with register address, "00h", to "17h". Then the following10 bytes contain its process lot and wafer information.

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

Memory Addr (Dec)	Memory Addr (hex)	SXGA120 R5 OLED Microdisplay
0	***0***	Serial Number Char #0
1	***1***	Serial Number Char #1
2	***2***	Serial Number Char #2
3	***3***	Serial Number Char #3
4	***4***	Serial Number Char #4
5	***5***	STAT
6	***6***	VINMODE
7	***7***	DISPMODE

8	***8***	TOPPOS
9	***9***	BOTPOS
10	***A***	RAMPCTL
11	***B***	RAMPCM
12	***C***	DAOFFSET
13	***D***	EXTRAMPCTL
14	***E***	Reserved
15	***F***	BIASN
16	***10***	GAMMASET
17	***11***	VCOMMODE
18	***12***	VGMAX
19	***13***	VCOM
20	***14***	IDRF
21	***15***	DIMCTL
22	***16***	TREFDIV
23	***17***	TEMPOFF
24	***18***	TUPDATE
25	***19***	TEMPOUT
26	***1A***	PWRDN
27	***1B***	TPMODE
28	***1C***	dTO

Memory Addr (Dec)	Memory Addr (hex)	SXGA120 R5 OLED Microdisplay
29	***1D***	Lot Char#0
30	***1E***	Lot Char#1
31	***1F***	Lot Char#2
32	***20***	Lot Char#3
33	***21***	Lot Char#4
34	***22***	Lot Char#5
35	***23***	Wafer Char#0
36	***24***	Wafer Char#1
37	***25***	Wafer Char#2
38	***26***	Wafer Char#3
39	***27***	Data Format Version# (01h)
40	***28***	VGNA0_HI
41	***29***	VGNA0_LO
42	***2A***	VGNA1_HI
43	***2B***	VGNA1_LO
44	***2C***	VGNA2_HI
45	***2D***	VGNA2_LO
46	***2E***	VGNA3_HI
47	***2F***	VGNA3_LO
48	***30***	VGNA4_HI
49	***31***	VGNA4_LO
50	***32***	VGNA5_HI
51	***33***	VGNA5_LO
52	***34***	VGNA6_HI
53	***35***	VGNA6_LO
54	***36***	VGNA7_HI
55	***37***	VGNA7_LO
56	***38***	VGNB0_HI
57	***39***	VGNB0_LO

Memory Addr (Dec)	Memory Addr (hex)	SXGA120 R5 OLED Microdisplay
58	***3A***	VGNB1_HI
59	***3B***	VGNB1_LO
60	***3C***	VGNB2_HI
61	***3D***	VGNB2_LO
62	***3E***	VGNB3_HI
63	***3F***	VGNB3_LO
64	***40***	VGNB4_HI
65	***41***	VGNB4_LO
66	***42***	VGNB5_HI
67	***43***	VGNB5_LO
68	***44***	VGNB6_HI
69	***45***	VGNB6_LO
70	***46***	VGNB7_HI
71	***47***	VGNB7_LO
72	***48***	GMMA00_HI
73	***49***	GMMA00_LO
74	***4A***	GMMA01_HI
75	***4B***	GMMA01_LO
76	***4C***	GMMA02_HI
77	***4D***	GMMA02_LO
78	***4E***	GMMA03_HI
79	***4F***	GMMA03_LO
80	***50***	GMMA04_HI
81	***51***	GMMA04_LO
82	***52***	GMMA05_HI
83	***53***	GMMA05_LO
84	***54***	GMMA06_HI
85	***55***	GMMA06_LO
86	***56***	GMMA07_HI

Memory Addr (Dec)	Memory Addr (hex)	SXGA120 R5 OLED Microdisplay
87	***57***	GMMA07_LO
88	***58***	GMMA08_HI
89	***59***	GMMA08_LO
90	***5A***	MM
91	***5B***	DD
92	***5C***	YY
93	***5D***	YY
94	***5E***	slope1 (int)
95	***5F***	slope2 (frac)
96	***60***	Intercept_low
97	***61***	Intercept_high