A SAMSUNG DISPLAY COMPANY

SXGA120-120 DESIGN REFERENCE BOARD

For Use with eMagin SXGA120 OLED Microdisplays

USER'S MANUAL

D01-500947-07

REVISION B

PART# EMA-200007

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1. INTRODUCTION

The SXGA120 Design Reference Board Rev. 5 provides the user with a highly compact, portable way of operating an eMagin SXGA120 OLED Microdisplay. This product was designed to deliver a complete tool for developers to evaluate and integrate eMagin SXGA120 microdisplays into new products. The included software package provides access to the microdisplay's on-board register settings from any Windows-based PC through a serial port.

2. FEATURES

- DVI Input
- RS-232 (serial) interface allows access to microdisplay registers
- Supporting Software (Windows)
- ON/OFF power switch

2.1. Software Features

- Read/write capabilities allow adjustments of microdisplay register settings to fine-tune image characteristics
- Software register control over the cathode voltage (Vcommon) input
- Software register control over the microdisplay's brightness
- Download and install new firmware files into your SXGA120 Design Reference Board for easy upgrades and expanded functionality
- Ability to read the microdisplay temperature
- Save feature stores custom register settings for convenience

3. SYSTEM REQUIREMENTS & SPECIFICATIONS

3.1. System Requirements

- For digital RGB inputs: A PC capable of producing a digital video output compliant with the DVI standard.
- Support software requires a Windows PC with an RS-232 serial port

3.2. SXGA120 Design Reference Board.

The SXGA120 Design Reference Board Rev. 5 is shown in figure 3-1 below. The major components are labeled for easier identification. The minimum requirements for displaying video on the SXGA120 Design Reference Board are; a +9 Volt power supply connected to the power connector, a digital video source connected to the HDMI connector (A DVI to HDMI adapter is included with the unit) and an SXGA120 OLED connected to the display connector (J12).
The SXGA120 Design Reference Board also supports eMagin Corporation's VGA microdisplay. However to do so requires a different on-board firmware and FPGA configuration, and the board can only support one configuration at a time. Please contact eMagin Corporation's Customer Service if you wish to change the DRK board to support the eMagin's VGA microdisplays.
As delivered with the SXGA120 Design Reference Kit, the board is configured to support SXGA120 displays only.

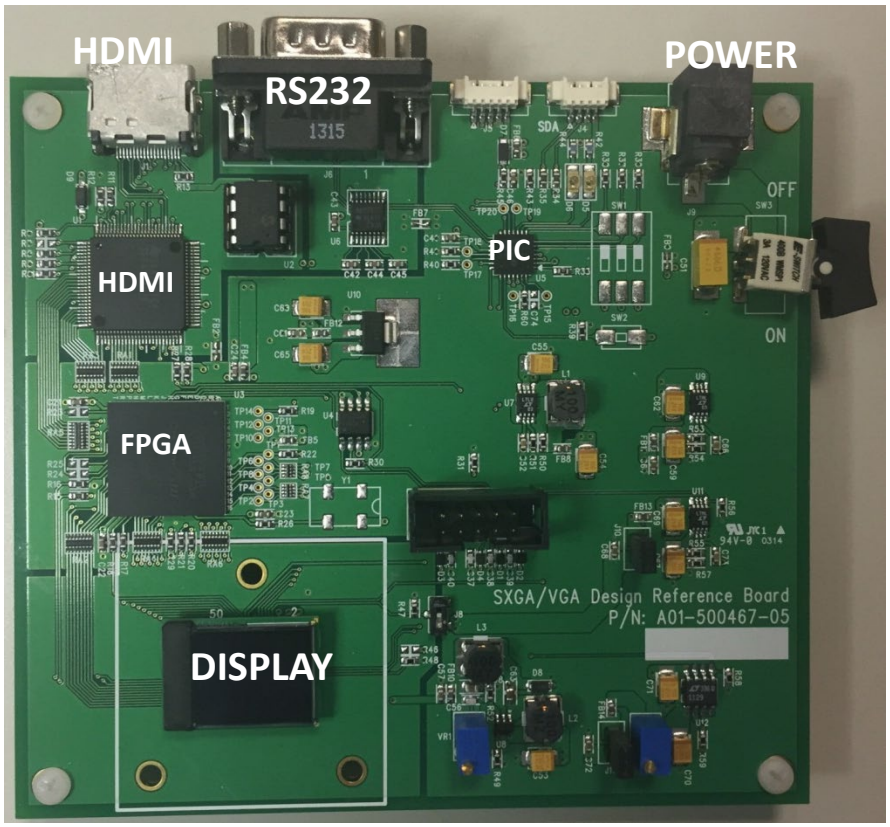
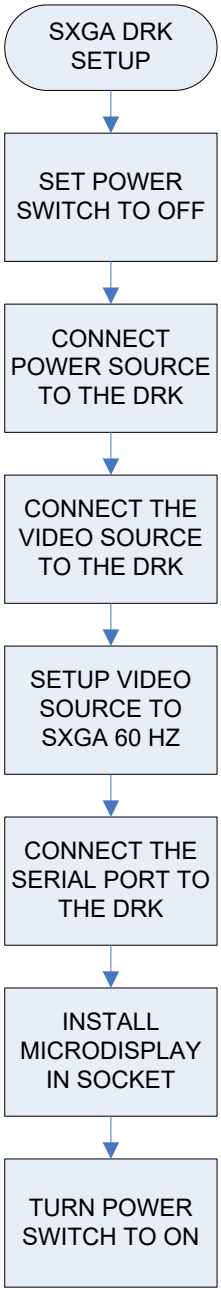


Figure 3-1 SXGA120 Design Reference Board Rev. 5

4. INTERFACE CONNECTIONS & SETUP

4.1. Setup Flow Chart



4.2. Connect Display to the Design Reference Board

The microdisplay connects to the Design Reference Board via a 50-pin board-to-board connector. The present version of the connector is **NOT** keyed so it is important to correctly orient the display. Refer to the picture below for the proper orientation. . The Display Carrier board is connected as shown in figure 4-1 below.

Note: The SXGA120 OLED can be damaged if it is not connected properly.

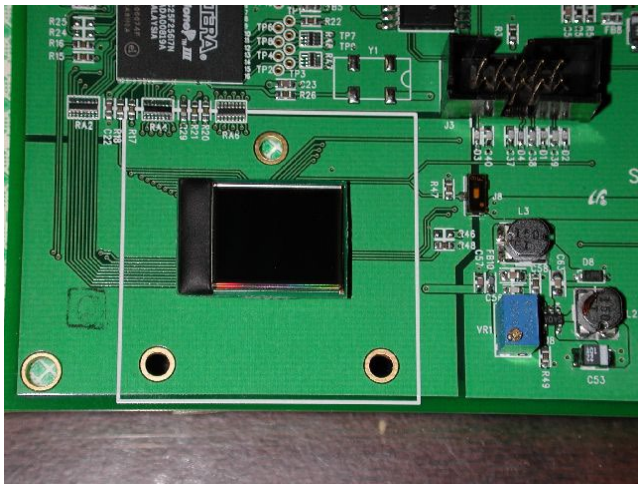


Figure 4-1 Display Carrier Board Connection Orientation

Lift the display by its sides and take care not to press on the active area or leave fingerprint marks on it. Insert the display into the Design Reference Board.

4.3. Setup PC for Proper Video Output

- The default compatible resolution is SXGA120 (1280x1024) with a refresh rate of 60 Hz. If you are using this input set the video resolution for 1280x1024 in your PC's display properties.
- Ensure that the refresh rate to set to 60 Hz, or other supported refresh rate per the display specification.
- If you are using a laptop PC, you may need to export the video signal to an external monitor. This is usually accomplished through a keypress including the Fn key + a designated function key. See your PC's operation instructions for more information.

4.4. Power Up

- Set the power switch to the ON position.

4.5. Power Down

- Set the power switch to the OFF position.

4.6. Brightness

eMagin strongly recommends that you drive the microdisplay at the minimum luminance necessary for your application. This will extend the lifetime of the display to its maximum possible lifetime. As OLED microdisplays are emissive devices, driving the microdisplay at high bias levels will decrease its overall lifetime.

5. USING THE SXGA120 DESIGN REFERENCE BOARD SOFTWARE

The SXGA120 Design Reference Board Rev. 5 includes a support software suite with the following functionality.

- Perform software microdisplay brightness adjustments
- Perform software adjustments of the Vcommon input to the microdisplay
- Read the microdisplay temperature
- Download and install new versions of the SXGA120 Design Reference Board firmware to update or provide new functionality using an RS-232 connection
- Read/write register values to the microdisplay and FPGA to control various characteristics (see your microdisplay User Specification for more information)

5.1. Jumpers and switch settings

The Design Reference board has two jumpers (J10 and J11) and one on-board slide switch (J8) that can be used to take power measurements and set the display in its burn-in (BI) mode. Refer to Figure 5.1 below for location.

Power Measurements
Jumpers J10 and J11 provide access the +2.5V and +5V display-only power rails. By removing the jumpers and connecting in series a current meter, it is possible to measure the display current draw from the +2.5V and +5V power supplies.

Burn-In Mode

Switch J8 is set by default to the non-Burn-In mode, as shown in Figure 5.1. Sliding the switch to the other position will configure the SXGA120-120 microdisplay in the Burn-In mode. Refer to the SXGA120-120 datasheet for details on this operational mode that allows the display to show a full flat field with all pixels on without having to have a valid input video connected.

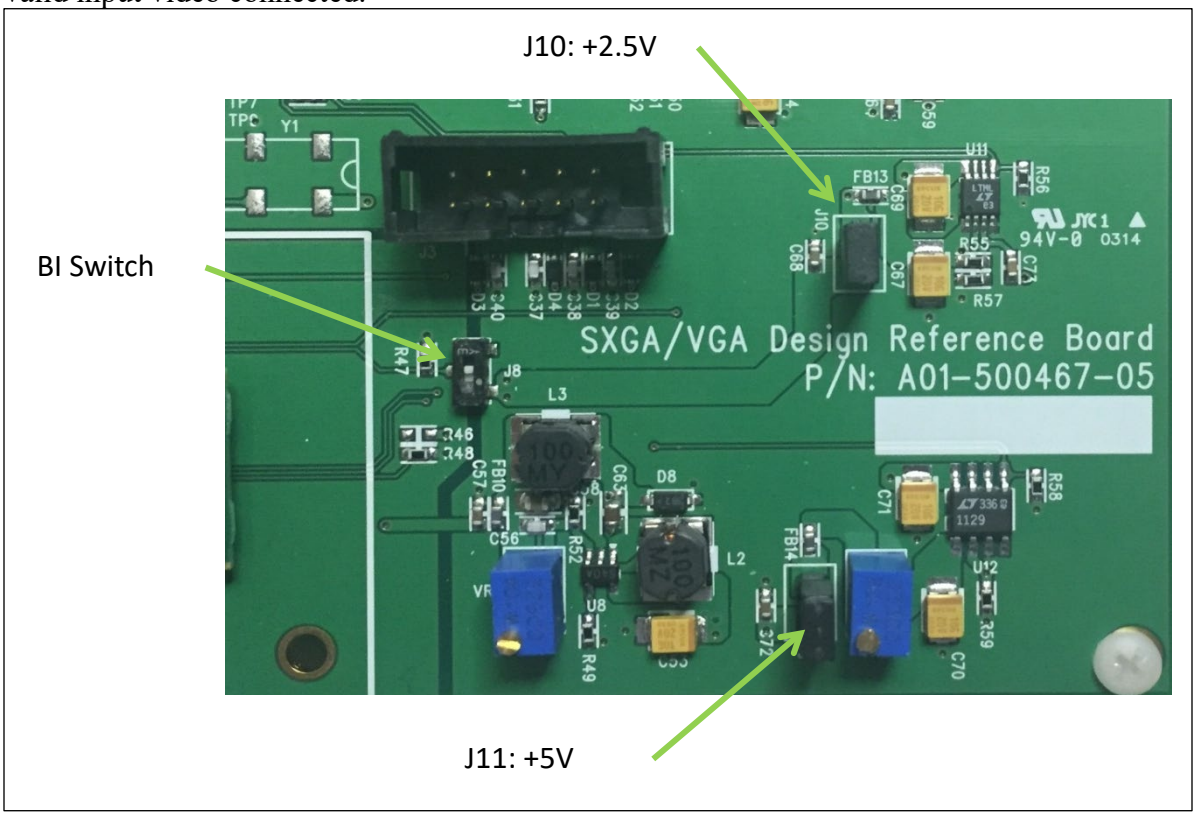


Figure 5.1 Jumper and switch location

5.2. Serial Interface Command Set

The SXGA120 Design Reference Board Rev. 5 can be controlled by sending commands and data using the included RS-232 cable. The software package includes a file called **S04-500491-00-SXGA_SW.exe** developed for this purpose.

5.3. SXGA120 Design Reference Board Software Utility

1. Connect the serial cable to the PC (Port 1) and to the RS232 connector on the SXGA120 Design Reference Board
2. Connect the power cable to the SXGA120 Design Reference Board
3. Connect the video source to the SXGA120 Design Reference Board
4. Turn on the SXGA120 Design Reference Board

5. Start the **S04-500491-00-SXGA_SW.exe** application and a screen should appear like that shown below:

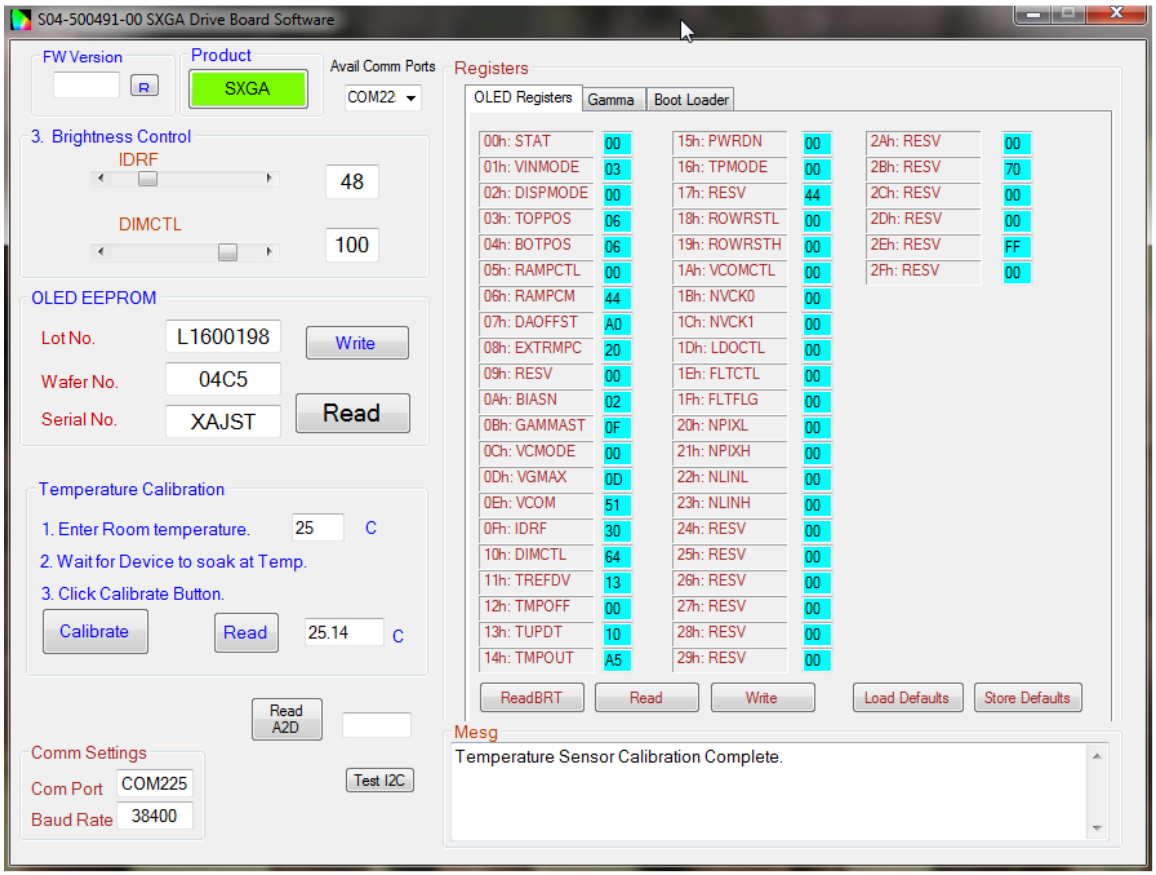


Figure 5-1 SXGA120 Design Reference Board Software Utility

6. The application communicates with the PIC microcontroller on the SXGA120 Design Reference Board and reads the initial status of the "OLED", "FPGA" and "VPG" shutdown pins.
7. The read/write buttons shown in the "OLED Registers" panel will read/write the register settings in their corresponding boxes from/to the OLED microdisplay.
8. The read/write buttons displayed in the "FPGA" panel will read/write the settings displayed in the register boxes from/to the SXGA120 Design Reference Board's FPGA.
9. The read/write buttons displayed in the "GAMMA" panel will read/write the values used in generating a Gamma table that resides in the FPGA

Direct control of the SXGA120 Design Reference Board can also be implemented into a customer specific application using the following hardware protocol and command set.

5.3.1. Hardware Protocol

- bit, no parity
- 38400 baud
- No hardware handshake

5.3.2.eMagin Software Command Set

TABLE 5-1 COMMAND SET LIST FOR ADDRESSING THE MICRODISPLAY REGISTERS

Command	Description
O	Select the OLED device Usage: O
F	Select the FPGA device Usage: F
E	Read the EEPROM device Usage: E Note: The E command is preceded by a HX command
J	Send a data value to the SXGA120 Design Reference Board Usage: JX where X = 0 to 255
H	Send a register value to the SXGA120 Design Reference Board Usage: HX where X = 0 to 255
W	Write a register Usage: W Note: The W command is preceded by a HX JY command
G	Change the Gamma Table Usage: GX where X = 0 to 3
P	Power down a device on the SXGA120 Design Reference Board Usage: PX where X = 0 to 7
Q	Returns the value at the A2D pin. Usage: Q Returns two values(high byte, low byte)
R	Read a register Usage: R Note: The R command is preceded by a HX JY command
S	Returns the status of a device on the SXGA120 Design Reference Board Usage: SX where X = 0 to 7
U	Update the Gamma lookup table in the FPGA. Usage: U

Note: The commands and values are typically generated from a control program. The values are sent in binary format to the Design Reference Board microcontroller, which will process these natively in binary. Below is an example write instance using the provided software:

In order to write the decimal value 81 to register 3, the following commands need to be issued: H3D81W

No space is required between the commands

Figure 5-1 Example microdisplay register value write using included software

5.4. Using Hyperterminal with the Design Reference Board

If you will use Hyperterminal to control the Design Reference Board please note that Hyperterminal converts all input data to ASCII characters. Therefore, the X value mentioned in the table above needs first to be converted to its ASCII equivalent in order to be recognized by the Design Reference Board firmware. Received information will also be displayed as ASCII code. An ASCII to decimal (or hexadecimal) conversion must be performed to read the correct values sent via the serial interface. We have provided an example write instance and ASCII character table for your reference.

To write the decimal value 81 to register 3, the following commands need to be issued: H CTRL-C D Q W Ctrl+C (pressing the Ctrl and C key simultaneously) is the ASCII equivalent of decimal 3 Note: No space is required between the commands. The spacing above is for clarity only.

Figure 5-2 Example microdisplay register value write using HyperTerminal

5.4.1.ASCII Table of Commands

TABLE 5-2 TABLE OF ASCII CHARACTER CODES

Non-Printing Characters					Printing Characters								
Name	Ctrl char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
null	ctrl-@	0	00	NUL	32	20	Space	64	40	@	96	60	`
start of heading	ctrl-A	1	01	SOH	33	21	!	65	41	A	97	61	a
start of text	ctrl-B	2	02	STX	34	22	"	66	42	B	98	62	b
end of text	ctrl-C	3	03	ETX	35	23	#	67	43	C	99	63	c
end of xmit	ctrl-D	4	04	EOT	36	24	$	68	44	D	100	64	d
enquiry	ctrl-E	5	05	ENQ	37	25	%	69	45	E	101	65	e
acknowledge	ctrl-F	6	06	ACK	38	26	&	70	46	F	102	66	f
bell	ctrl-G	7	07	BEL	39	27	'	71	47	G	103	67	g
backspace	ctrl-H	8	08	BS	40	28	(	72	48	H	104	68	h
horizontal tab	ctrl-I	9	09	HT	41	29	)	73	49	I	105	69	i
line feed	ctrl-J	10	0A	LF	42	2A	*	74	4A	J	106	6A	j
vertical tab	ctrl-K	11	0B	VT	43	2B	+	75	4B	K	107	6B	k
form feed	ctrl-L	12	0C	FF	44	2C	,	76	4C	L	108	6C	l
carriage feed	ctrl-M	13	0D	CR	45	2D	-	77	4D	M	109	6D	m
shift out	ctrl-N	14	0E	SO	46	2E	.	78	4E	N	110	6E	n
shift in	ctrl-O	15	0F	SI	47	2F	/	79	4F	O	111	6F	o
data line escape	ctrl-P	16	10	DLE	48	30	0	80	50	P	112	70	p
device control 1	ctrl-Q	17	11	DC1	49	31	1	81	51	Q	113	71	q
device control 2	ctrl-R	18	12	DC2	50	32	2	82	52	R	114	72	r
device control 3	ctrl-S	19	13	DC3	51	33	3	83	53	S	115	73	s
device control 4	ctrl-T	20	14	DC4	52	34	4	84	54	T	116	74	t
neg acknowledge	ctrl-U	21	15	NAK	53	35	5	85	55	U	117	75	u
synchronous idel	ctrl-V	22	16	SYN	54	36	6	86	56	V	118	76	v
end of xmit block	ctrl-W	23	17	ETB	55	37	7	87	57	W	119	77	w
cancel	ctrl-X	24	18	CAN	56	38	8	88	58	X	120	78	x
end of medium	ctrl-Y	25	19	EM	57	39	9	89	59	Y	121	79	y
substitute	ctrl-Z	26	1A	SUB	58	3A	:	90	5A	Z	122	7A	z
escape	ctrl-[	27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
file separator	ctrl-\	28	1C	FS	60	3C	<	92	5C	\	124	7C	|
group separator	ctrl-]	29	1D	GS	61	3D	=	93	5D	]	125	7D	}
record separator	ctrl-^	30	1E	RS	62	3E	>	94	5E	^	126	7E	~
unit separator	ctrl-_	31	1F	US	63	3F	?	95	5F	_	127	7F	DEL

5.5. Downloading New Firmware Versions to the Design Reference Board

The ability to download new versions of the firmware ensures that you will have the latest functionality without having to send your SXGA120 Design Reference Board for reprogramming. A utility that downloads and installs new firmware versions is included in the software package.

5.5.1. Using the Firmware Download Utility

Firmware files can be downloaded as hex files. Before attempting to download and install new firmware versions make sure that you have received a firmware hex file from an eMagin source.

To load your firmware files, follow the following steps:

1. Connect the serial cable to the PC and to the RS232 connector on the SXGA120 Design Reference Board
2. Connect the power cable to the SXGA120 Design Reference Board.
3. Connect your video source to the SXGA120 Design Reference Board.
4. Start the **S04-500491-00-SXGA_SW.exe** application. Select the "Bootloader" menu at the top of the form. A window should appear like that below:

Figure 5-3 Firmware download utility

5. Make sure the following settings are shown
   a. Processor = 18F2523
   b. Com Port = 1

6. Click the "Program" button to find the hex file you wish to install. **Note: The power on the SXGA120 Design Reference Board should be off while setting up your download. Only turn on the power to the SXGA120 Design Reference Board when you are ready to write your new firmware to the PIC.**

7. When you turn on the SXGA120 Design Reference Board, the hex file should begin to upload. The progress bar will turn blue.
8. When the upload is complete, the SXGA120 Design Reference Board will run.

6. ADVANCED USER INFORMATION

6.1. Microcontroller

The SXGA120 Design Reference Board utilizes a Microchip PIC18F2523 microcontroller. This is a CMOS Flash microcontroller in a 28 pin package. Provisions are on the circuit board for in circuit reprogramming but are not accessible without opening the case. Please refer to the Microchip PIC18F2523 datasheet available from Microchip Technology Inc. for additional information about the microcontroller and programming.

The main function of the microcontroller is to communicate with the OLED display and the FPGA. All communication is over the internal I^2C bus and the microcontroller acts as the bus master. On power up the registers of the OLED and FPGA are initialized with the default settings programmed into the microcontroller. After initialization the microcontroller scans for user input and monitors the OLED and FPGA.

6.2. I^2C bus

The microcontroller is the bus master and communication occurs at the standard 100 KHz clock rate. The microcontroller, the OLED and the FPGA all operate from 2.5VDC so the I^2C bus must also operate using 2.5V logic levels. The maximum speed allowed for I^2C bus communication is 400 KHz. Please refer to the Philips I^2C bus specification available on the Philips website for detailed information.

6.3. System Hardware Overview

Figure 6-1 below is a block diagram of the main functions on the SXGA120 Design Reference Board.

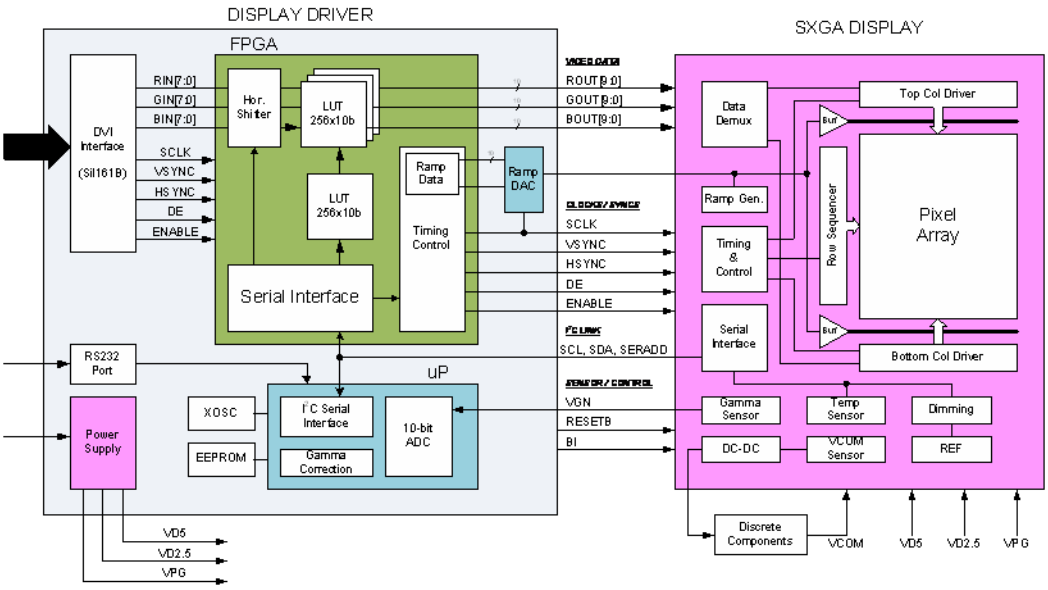


Figure 6-1 System level Block Diagram

6.4. **Voltages**

The power supply section of the SXGA120 Design Reference Board consists of several voltage regulators, some of which are adjustable with potentiometers. Table 6-2 below describes the voltages and there purpose.

Voltage	**Range**	**Typical**	**Purpose**
Vinput	+6.0 Volts to +7Volts	+6.5Volts	Main Supply
V5	5Volts ±10% (fixed)	5 Volts	LEDS, DAC
V3.3	3.3Volts ±10% (fixed)	3.3 Volts	DVI, RS232
V2.5	2.5Volts ±10% (fixed)	2.5 Volts	FPGA, OLED
VAN	5.0V (adjustable with pot)	5.0 Volts	OLED Anode
VPG	-1.5V (adjustable with pot)	-1.5V	OLED Bias
VDD	2.5V ±10% (fixed)	2.5V	OLED

Table 6-2 shows the voltage and current relationship at power-on.

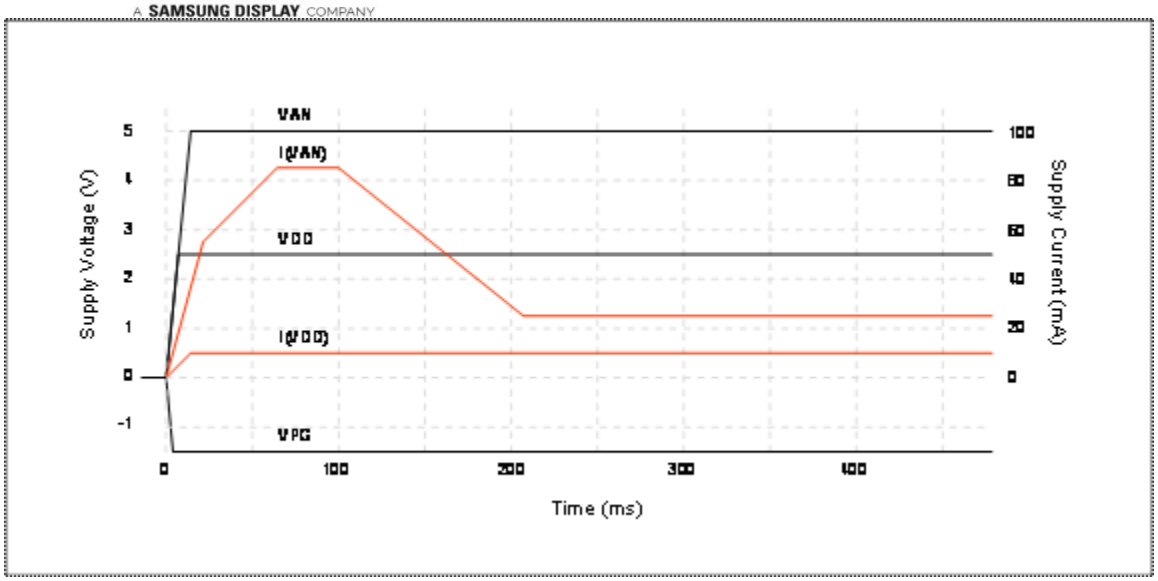


Figure 6-2 SXGA120 Power On

6.5. Bias Control

BIASN: Normal board – BIASN=2 gives the best results.

6.6. VCom Mode

VCOMMODE:
Dimming: use register VCOM to set brightness level in Manual mode. The chart below shows Luminance vs. Manual VCOM for a color SXGA120 display.

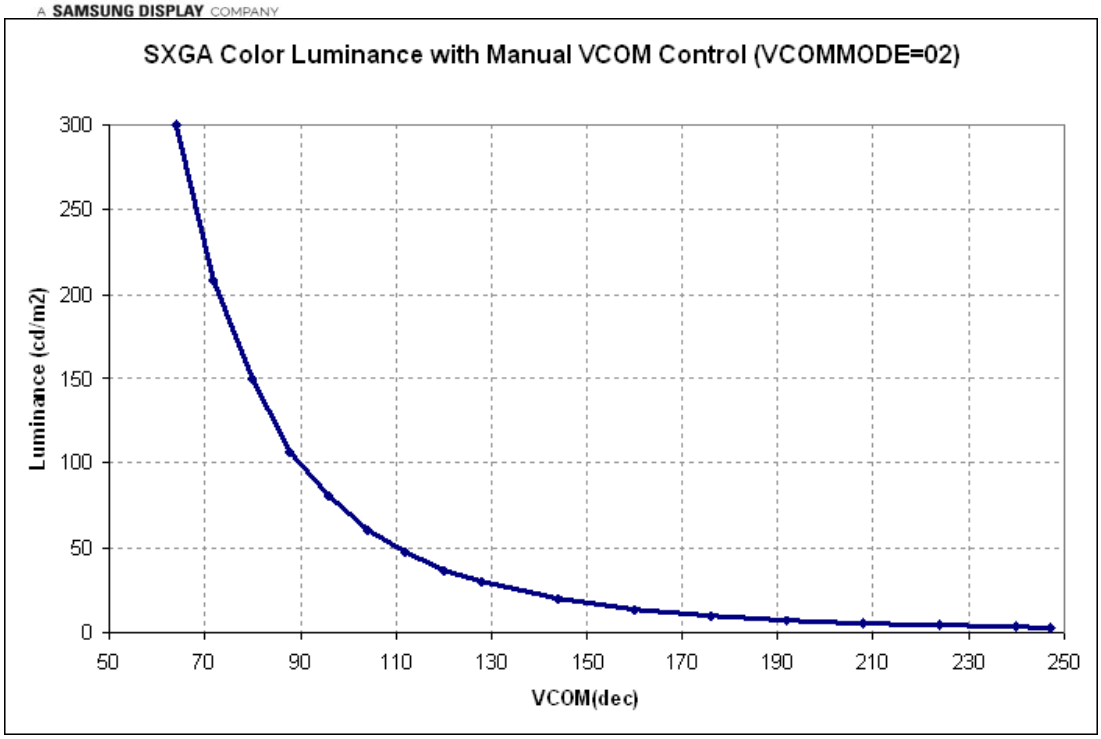


Figure 6-4 Luminance vs Manual Vcom

6.7. Gamma

To compensate for the non-linear dependency of luminance on the voltage of the OLED diode, the R, G and B signals include internal gamma correction to linearize the pixel response as a function of the input video signal. This gamma correction takes place in the FPGA.

The gamma correction consists of a nine segment piece-wise-linear function whose parameters are set from the pull-down menu or via registers in the "Gamma" panel on the windows software. All three color channels have the same PWL shape.

There are multiple ways to set the Gamma using the windows software. The Gamma section of the software is shown below.

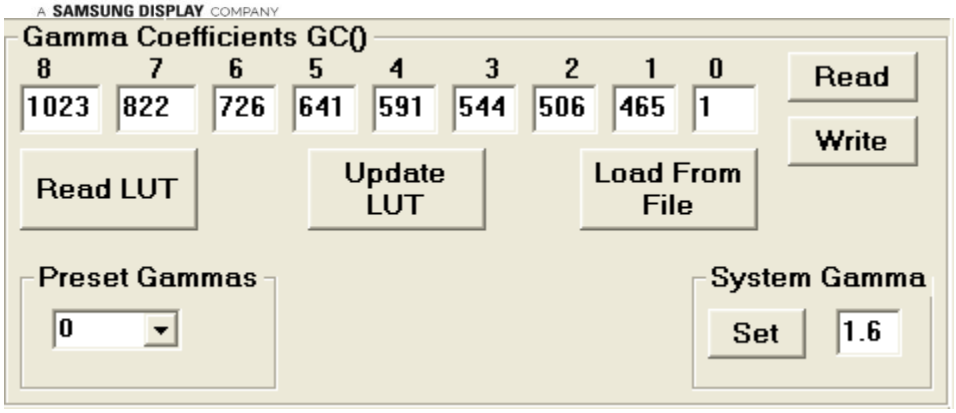


Figure 6-5 The Gamma Section of the Software

6.7.1.Gamma Coefficients GC(0-8)

The 9 boxes in the Gamma section represent the 9 segment piece-wise-linear function that defines the gamma curve. These 9 values are used to calculate the 256 element look-up-table (LUT) that is required to transform input video data into a gamma-corrected data signal for the microdisplay input port. The "Read" button will retrieve the current 9 values from the microcontroller. The user can change any of the 9 values and see the resulting gamma corrected video by pressing the "Write" button.

6.7.2.Preset Gamma Table descriptions

There are 3 Gamma tables programmed into the Microcontroller firmware and can be selected from the windows software. They can be selected by using the pull-down menu in the lower left of the Gamma section. (Preset GAMMAS) Each table was calculated for a linear response at different luminance levels. For instance, Table 0 is for low luminance applications.

6.7.3.Using "Update LUT" Button for Auto-Gamma Correction

The software allows for the immediate update of the gamma tables with the push of a button, "Update LUT". This button, located in the center of the software form, tells the firmware to calculate the Gamma coefficients using the VGN signal provided by the SXGA120 microdisplay. This feature allows the display gamma to be automatically adjusted for any operating conditions of temperature and brightness. The firmware calculates the 9 Gamma coefficients and then the full 256 value lookup table. This lookup table is then loaded, by the firmware, into the FPGA.

6.7.4.Loading the LUT from a file

The software allows for the loading of the gamma tables from a text file. The format is as follows;

1
174
396
529
575
583
591
599
607
612
618
.
.
1023

Each of the 256 values is on a separate line. This lookup table is then loaded, by the firmware, into the FPGA. There are 3 files shipped with the software package.

6.7.5.The “Read LUT” Button

The software allows for the reading of the full 256 values of the LUT using this button. The result is displayed in the message box at the bottom of the software. The user can scroll through all the values or select and save to a text file. These LUT values are the values before being gray-coded.

6.7.6.System Gamma

The software allows for the overall System Gamma to be set between 0.5 and 2.5 when using the Auto-Gamma feature. This System Gamma can be used to compensate for the gamma of the input video. For example, if the source video is gamma corrected to 2 then setting the System Gamma to 1.9 and pressing the “Set” button and then the “Update LUT” button will give a better overall gamma response. This does not mean that there is a 1 to 1 relationship between input gamma and the System Gamma.

Figures 6-6 to 6-8 show the grayscale response for a display at several luminance settings obtained by using the “Update LUT” feature and the System Gamma set to 1.

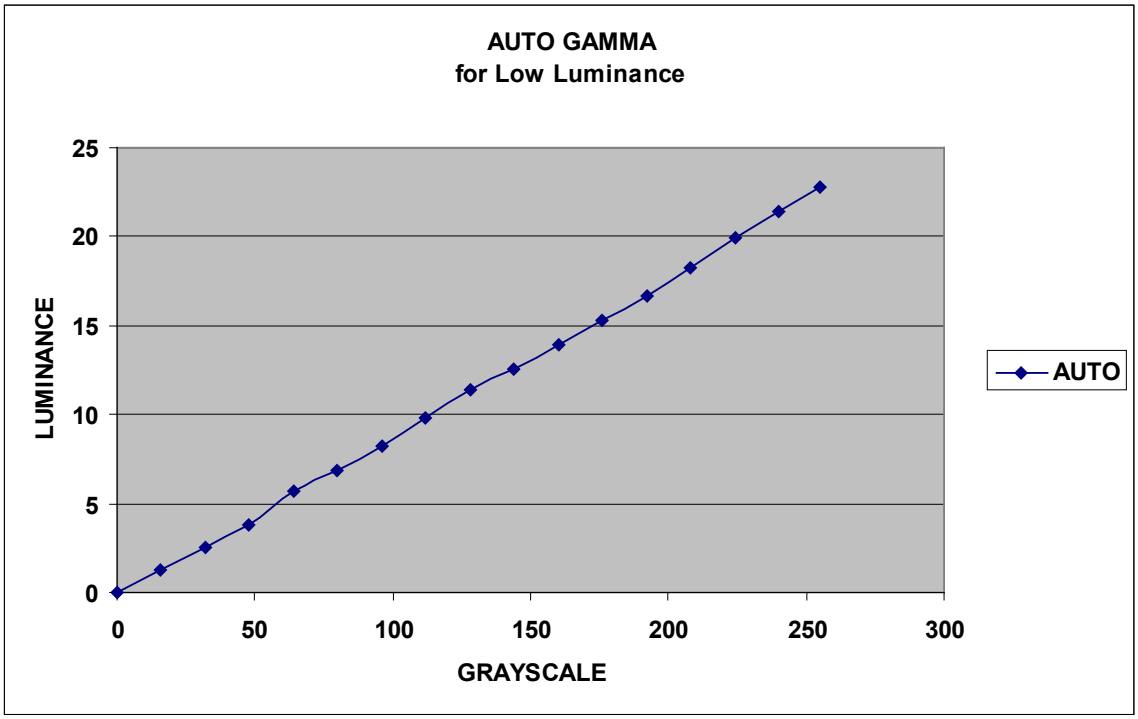


Figure 6-6 Luminance Response for Auto Gamma at Low Luminance

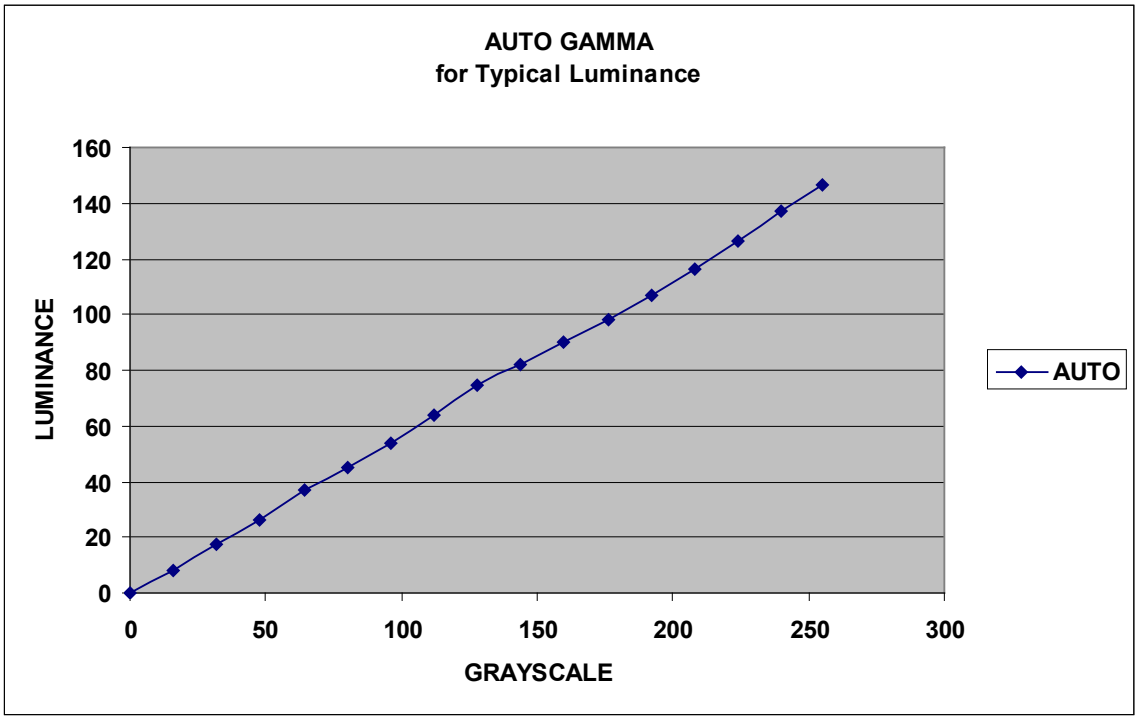


Figure 6-7 Luminance Response for Auto Gamma at Typical Luminance

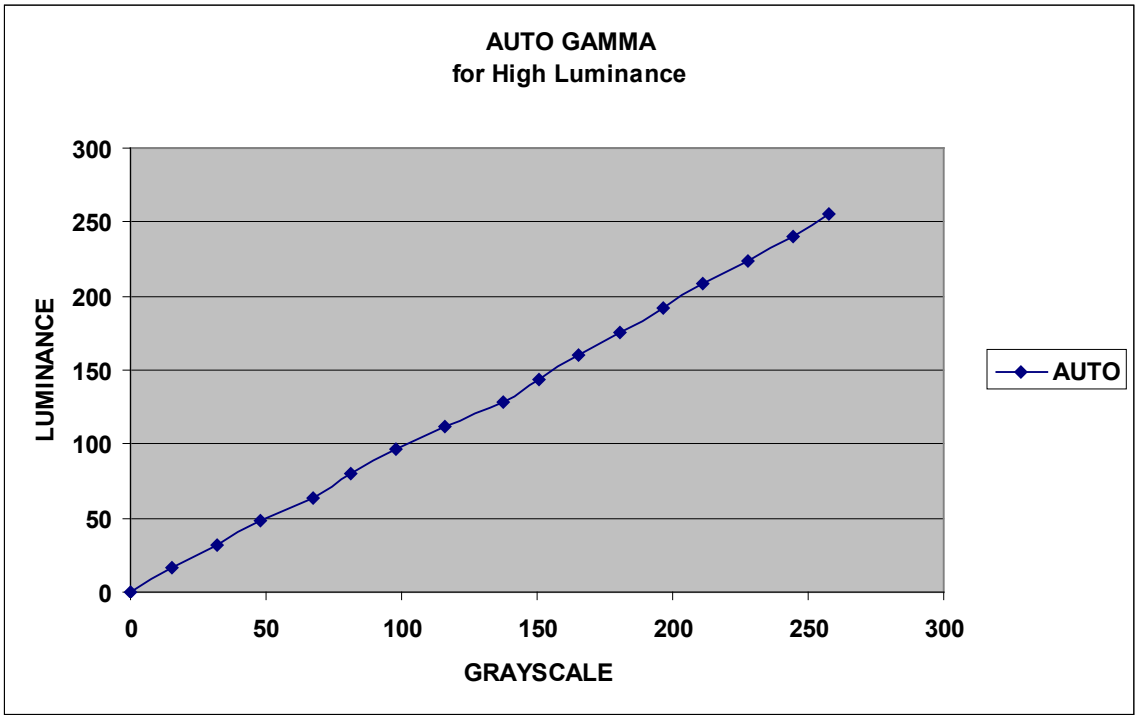


Figure 6-8 Luminance Response for Auto Gamma at High Luminance

6.8. Temperature Read

Temperature read – not calibrated to actual temperature.

6.9. Calculating DAOFFSET

Registers DAOFFSETH and DAOFFSETL are used to adjust the maximum value of the internal RAMP DAC signal. DAOFFSETH can increase the maximum level by up to +20% and DAOFFSETL can decrease the maximum level by up to -20% of the nominal value.
The typical dependence of display luminance on DAOFFSET is shown in Figure 6.6. The luminance is seen to saturate for DAOFFSET greater than 20 in this sample. For normal operation DAOFFSET should be set to a value just below the saturation region. It should be adjusted for an operating luminance equal to 84-91% of the saturated or maximum value.

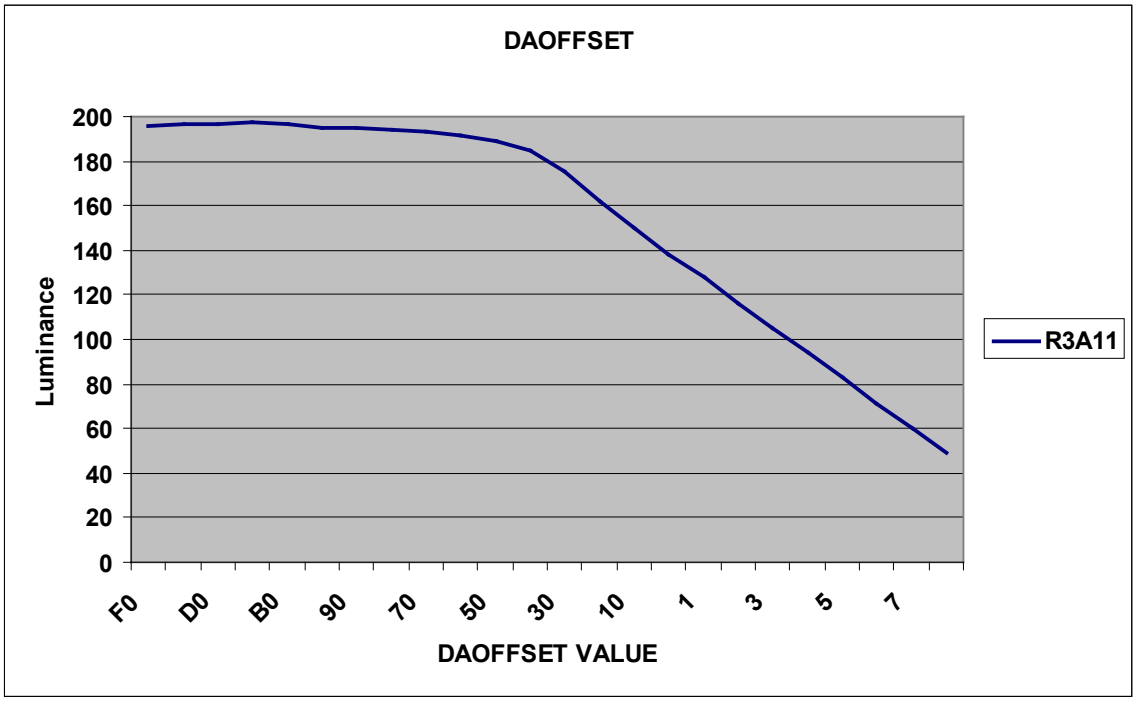


Figure 6-9 Luminance vs DAOFFSET register value.

Follow these steps to determine DAOFFSET for each display.

(Use default settings for registers VCOMMODE=00, IDRF=30h, DIMCTL=64h)

1. Set the DAOFFSET register to 0xF0 and measure luminance. (eg. 100cd/m2)
2. Calculate 91% of the measured luminance. (eg. 91cd/m2)
3. Set the DAOFFSET register to 0x10 and measure luminance.
    a. If the measured luminance for DAOFFSET=0x10 is greater than 91% of DAOFFSET=0xF0 then the DAOFFSET value is less than 0x10.
    a. If the measured luminance for DAOFFSET=0x10 is less than 91% of DAOFFSET=0xF0 then the DAOFFSET value is greater than 0x10.
4. Continue adjusting the DAOFFSET register until the measured luminance is approximately equal to 84 - 91% of DAOFFSET=0xF0.

7. FPGA

7.1. FPGA Register Map

I2C Slave Address : 010110X						
Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STATE	R	REV	2-0	0	Silicon Revision Number
01	VIDMODE	R/W	CKOPOL	7	0	Clock out polarity 0 = positive edge, 1 = negative edge
			RESERVED	6	0	Do not use
			INTER	5	0	Interlaced video enable 0 = progressive video, 1 = Interlaced video
			DVGA	4	0	Input video resolution 0 = SXGA, 1 = DVGA
			STARTX	3-0	6	Line data start position (range 0 to C)
02	ADDR	R/W		7-0	0	Write address for LUT template
03	WRDATA	R/W	WRDATA[7:0]	7-0	0	Write LSB data for LUT template with WRDATA write and auto address increment
04			WRDATA[9:8]	1-0	0	Write MSB date for LUT template
05	LUTRDY	R/W	LUTRDY	0	0	LUT update ready flag (LUT template write disable when "1") 0 = LUT not ready, 1 = New LUT is ready for update
06	SYNCPOL	R/W	VSPOL	1	1	VSYNC polarity 0 = negative sync, 1 = positive sync
			HSPOL	0	1	HSYNC polarity 0 = negative sync, 1 = positive sync
07	RAMPCTL	R/W	RAMPEN	6	0	Ramp generator enabl 0 = disable, 1 = enable
			RAMPST	5-0	20	Ramp start position (16 SCLK to 48 SCLK after HSYNC rising edge) 10=16 SCLK, 11=17 SCLK, … 20=32 SCLK, … 30=48 SCLK

8. REVISION HISTORY

Revision Level	ECN	Date	Description
1		07/23/08	Initial Release
2		08/14/08	Included new software features. (Gamma Table)
3		10/21/08	New Rev. 2 Drive Board
4		9/10/09	Updated Software Version Number.(V1.4 to V1.6)
5		2/18/2010	New Gamma Functions added.
6		12/17/2010	Updated FPGA Register Map
7		3/27/2015	Added jumpers and slide switch description (p 5 & 6)
A	000904	01/28/2020	Changed SXGA to SXGA120. Misc typo corrections
B	CF-000107	5/13/2024	Updated Logo “eMagin SDC”