SXGA-096 MW XLS

1280 X 1024 LOW-POWER MONOCHROME WHITE AMOLED MICRODISPLAY

DATASHEET
Revision -

For Part Numbers:

EMA-101205-01

eMagin Corporation 700 South Road, Suite 201 Hopewell Junction , New York 12533 www.emagin.com

Revision Level	ECN	Date	Scope
-		2022	Initial Release

TABLE OF CONTENTS

1. INTRODUCTION

The SXGA-096 Monochrome White OLED-XLS device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high brightness, high resolution, high image quality, compact size, and low power. Combining a total of 4,015,536 active dots, the SXGA-096 display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XLS technology offering extended life and luminance performance.

The active array is comprised of 1292 x 1036 square pixels with a 9.6-micron pitch and a 75% fill factor. An extra 12 columns and 12 rows (beyond the 1280 x 1024 main array) are provided to enable the active SXGA-096 display to be shifted by steps of 1 pixel in the X and Y directions for optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 3.2 x 9.6 micron identical sub-pixels, which together form the 9.6-micron square WHITE pixel group. Since the cmos circuitry is designed to support color through 3 independent data paths, this document will occasionally mention color. However, the EMA-100205-01 has a white OLED stack and cannot render colors. As a result, it is best to use identical data values for all 3 data paths, or configure the display for monochrome mode which can help reduce power by reducing the number of required LVDS pairs.

The SXGA-096 design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. In addition to its flexible matrix addressing circuitry, the SXGA-096 includes an internal 10-bit DAC that ensures 256 fully gamma-corrected gray levels, an on-chip set of look-up-tables for digital gamma correction, and a novel pulse-width-modulation (PWM) function that, together with the standard analog control, provides an extended dimming range. The PWM function also enables an impulse drive mode of operation that significantly reduces motion artifacts in high speed scene changes.

The SXGA-096 includes a very low-power, low-voltage-differential-signaling (LVDS) serialized interface for video data transport that minimizes the number of board interconnections and connector size, reduces electromagnetic emissions (EMI), and enables a lightweight and flexible cable link to a remote video source. Compatibility with standard LVDS drivers found in most commercially available FPGAs simplifies the system integrators task.

Detailed device specifications and application information for the SXGA-096 OLED-XLS microdisplay produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION

2.1 SXGA-096 WHITE XLS Microdisplay

Display Type:	Emissive, WHITE XLS AMOLED on Silicon
Format:	1280(x3) x 1024 pixels
Total Pixel Array:	1292(x3) x 1036 pixels
Pixel Size & Aspect Ratio:	9.6-micron Square
Fill Factor	75%
Viewing Area	12.4 x 9.945 mm (15.9 mm diagonal (0.62"))
Mechanical Envelope	20.0 x 16.5 x 5.0 mm (w x l x h)
Weight	<3 gm.
Gray Levels	256 levels per primary WHITE
Uniformity	> 85% end-to-end uniformity
Pixel Spatial Noise	<5% (1 sigma)
Contrast Ratio	>10,000:1 (at maximum luminance)
Pixel Response	Linear with input video signal (using internal gamma LUT)
Dimming Ratio	>200:1 analog, >200:1 pwm, >4,000:1 total (maximum)
White Luminance	4,100 cd/m^2 typical
CIE (White)	CIE-X = 0.30 to 0.36, CIE-Y = 0.37 to 0.42
Video Modes	SXGA, HD720, DVGA, 8-bit control of active window Progressive & Interlaced scan Horizontal (left/right) and vertical (up/down) scan control Horizontal and vertical image shift by up to 12 pixels
Video Interface	Serialized LVDS, 24-bit Digital RGB (up to 5 twisted line pairs including the clock pair)
Refresh Rate	30 to 85 Hz
Video Source Clock	120 MHz max
LVDS Clock	480 MHz max
LVDS Data Rate	960 Mbps
Control Interface	I^{2}C serial interface (+1.8VDC)
Power Consumption	~ 380 mW typical @ 1,500 cd/m^2 (Ta=+20°C)
Power Supply	
VDD5 (analog & array)	5VDC ±5% (250 mA maximum)
VDD1.8 (logic & I/Os)	1.8VDC ±5% (20 mA maximum)
VPG	-1.5VDC ±5% (1 mA maximum)
Operating ambient temperature	-46 to +71°C
Storage temperature	-55 to +85°C
Humidity	85%RH non condensing

3. FUNCTIONAL OVERVIEW

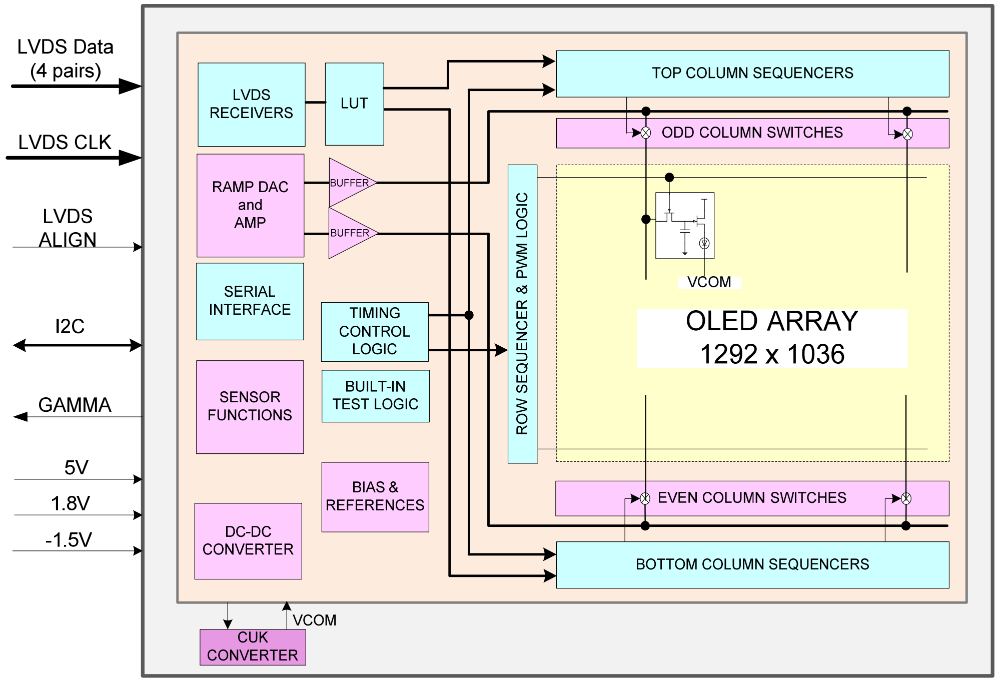


Figure 1: Top-level block diagram for SXGA-096

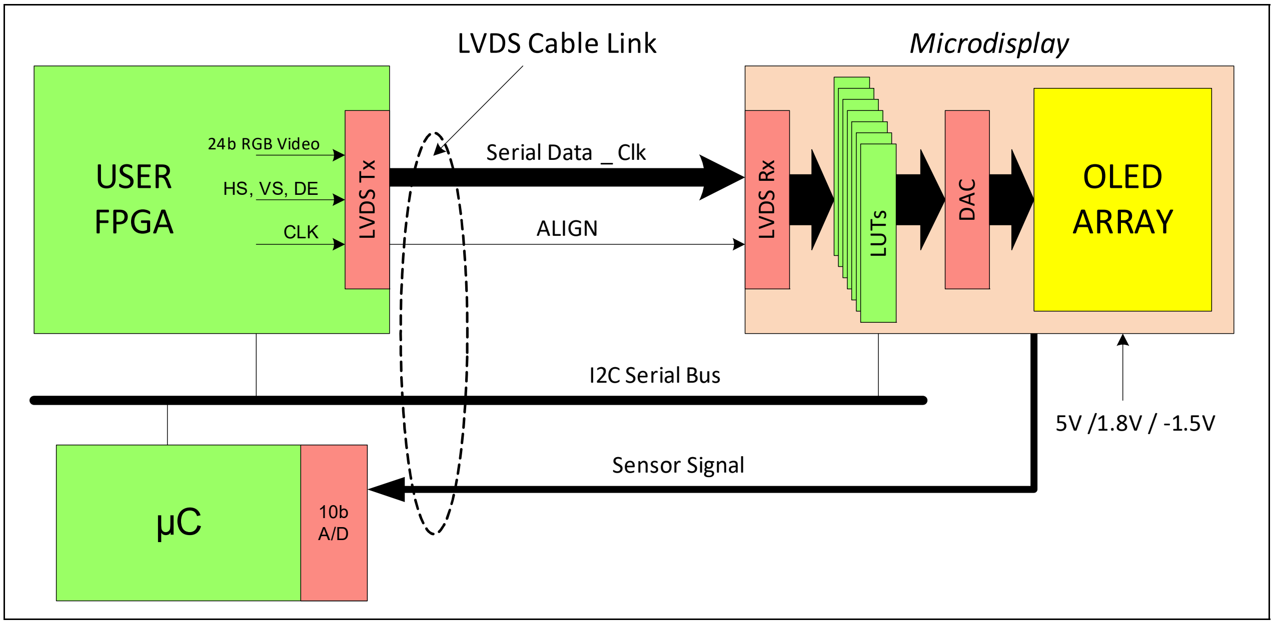


Figure 2: System application diagram

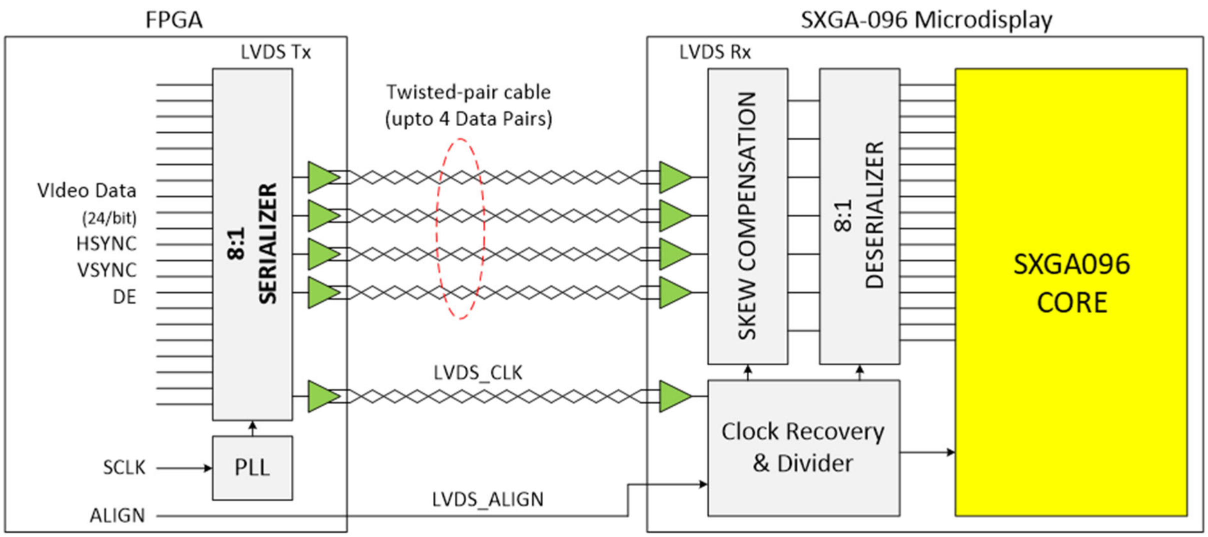


Figure 3: LVDS interface diagram

4. INPUT / OUTPUT DESCRIPTION

Connector J1 is a Hirose DF12NB(3.0)-30DP-0.5V(51) or DF12D (3.0)-30DP-0.5V (obsolete as of 12-31-2021)

Connector J1

Pin #	Pin Name	Type	Description
1	GND	Power	Power return terminal.
2	VPG	Power	Negative voltage bias for array protection switch. (-1.5 V)
3	RD3P	LVDS	LVDS Digital Data and Sync Input Port.
4	GND	Power	Power return terminal.
5	RD3N	LVDS	LVDS Digital Data and Sync Input Port.
6	VDD5	Power	Input power for Analog Circuits (5VDC).
7	GND	Power	Power return terminal.
8	VDD5	Power	Input power for VCOM (5VDC).
9	RD2N	LVDS	LVDS Digital Data and Sync Input Port.
10	VDD5	Power	Input power for Pixel Array (5VDC).
11	RD2P	LVDS	LVDS Digital Data and Sync Input Port.
12	GND	Power	Power return terminal.
13	GND	Power	Power return terminal.
14	VDD1.8	Power	Input power for logic and I/O pads.
15	RCKN	LVDS	LVDS source clock.
16	VGN	Analog Out	Gamma sensor output signal. (0 to +2.5V)
17	RCKP	LVDS	LVDS source clock.
18	BURN_IN	Logic In	Activates test mode used for Burn-In.
19	GND	Power	Power return terminal
20	RESETB	Logic In	Asynchronous system reset (active low).
21	RD1N	LVDS	LVDS Digital Data and Sync Input Port.
22	ENABLE	Logic In	Enable logic input.
23	RD1P	LVDS	LVDS Digital Data and Sync Input Port.
24	SCL	Logic In	Clock port for the serial interface. 400 KHz Max.
25	GND	Power	Power return terminal
26	SDA	Logic I/O	Data port for the serial interface. Open collector I/O
27	RD0N	LVDS	LVDS Digital Data and Sync Input Port.
28	SERADD	Logic In	Serial interface LSB address bit. Must be connected.
29	RD0P	LVDS	LVDS Digital Data and Sync Input Port.
30	LVDS_ALGN	Logic In	LVDS logic initialization signal (CMOS input).

5. PIXEL ARRAY LAYOUT

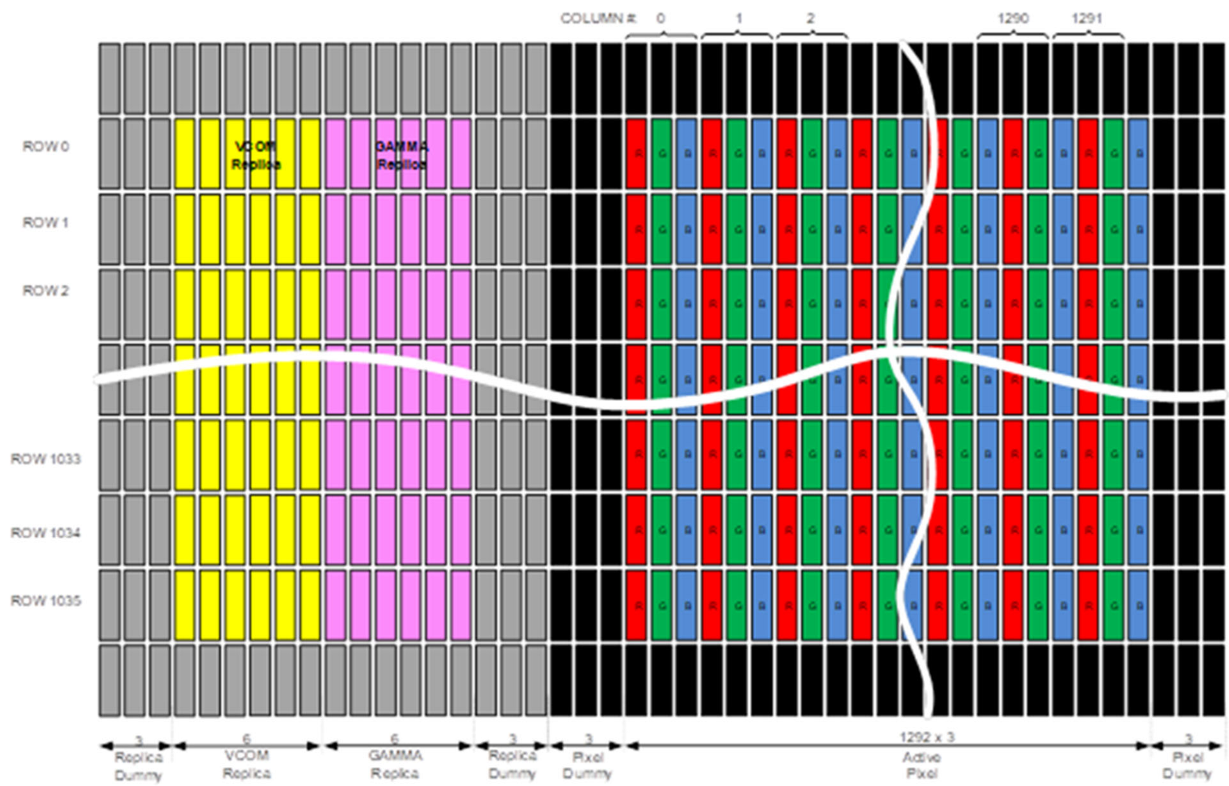


Figure 4 Pixel arrangement

6. ELECTRICAL CHARACTERISTICS

Table 6-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	-0.3		2.5	VDC
VDD5	Array/Analog Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3		0	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-45		+125	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 6-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	1.71	1.8	1.89	VDC
VDD5	Array/Analog Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-45	+25	+70	°C
Pdt	All Pixels On Power Consumption (+25°C)		700	1,000	mW

Table 6-3 : DC Characteristics

(Ta = 20°C, VDD1.8 =+1.8V, VDD5 = +5V, GND = 0V)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply		1.8		V
VDD5	Array/Analog Power Supply		5		V
VCOM	Common electrode bias	-6	-1.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		0.6	V
Vih	Digital input high level	1.2		VDD1.8+0.3	V
Vol	Digital output low level		GND	0.5	V
Voh	Digital output high level	VDD1.8-0.2	VDD		V
VGN	Gamma feedback signal	0		5	V

Table 6-4 : AC Characteristics

(Ta = +20°C, GND = 0V, VDD1.8= +1.8V, VDD5 = +5.0V, VPG = -1.5V,)

Symbol	Parameter	Min	Typ.	Max.	Unit
SCLK	Video Clock Frequency	44	-	120	MHz
CLK_Duty	SCLK duty cycle	45		55	%
Fhs	Horizontal Sync frequency	30		70	KHz
Fvs	Vertical Sync Frequency	30		85	Hz
Tlo	Line Overscan (% of line time)	3			%
Tfb	Frame Blanking (% of frame time)	1			%
Trst	Reset Pulse Width	100		-	µs
Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VDD5	Average VDD5 Power Consumption (SXGA Mode 60 Hz refresh rate)		400		mW
Pd VDD1.8	Average VDD1.8 Power Consumption (SXGA Mode 60 Hz refresh rate)		30		mW
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode		2.5		mW
Ta	Ambient Operating Temperature	-46		+71	°C

Power consumption measured at 60Hz refresh rate, room ambient temperature and with a TV-like WHITE test pattern that represents an average video mode (See below Figure 5) and a full white field equivalent luminance of 1,500 cd/m^2

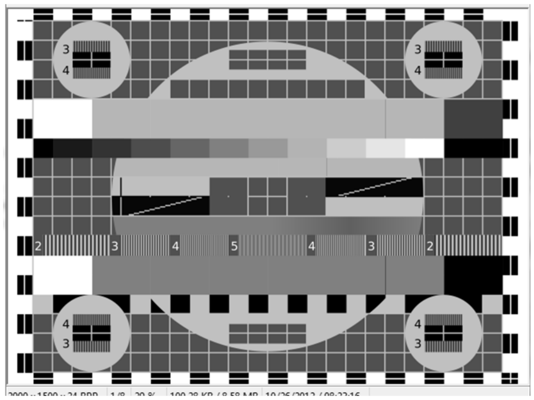


Figure 5: WHITE Test Pattern

Figure 6 shows the typical room temperature power consumption of the display vs. luminance with all pixels on at maximum gray level.

Figure 6: SXGA096 CFXLS Power vs. Luminance

Figure 7 shows the typical power consumption (mW) over the operational temperature range (°C) and a room temperature luminance set to 4100 cd/m^2 with 50% of the pixels turned on.

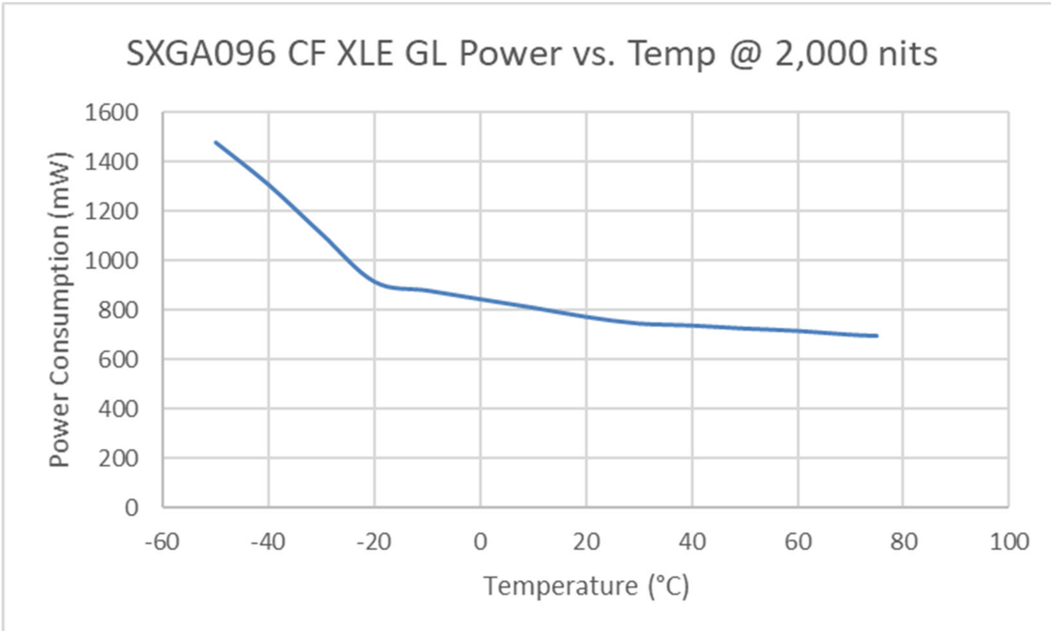


Figure 7: Power vs. Temperature

6.1 Timing Characteristics

6.1.1 LVDS Inputs Characteristics

Applies to RD0P, RD0N, RD1P, RD1N, RD2P, RD2N, RD3N, RD3P, RCKP, RCKN signals

(Ta = 25°C, VDD1.8 =+1.8V, VDD5 = +5V, VOLED = -7V, GND = 0V)

Symbol	Parameter		Min	Typ.	Max.	Unit
V_{CM}	Common Mode Input Range			1.2		V
V_{TH}	Differential Input High Threshold. V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold. V_{CM} = +1.2V		-100			mV
I_{IN}	Input Current	V_{IN} = 1.8V		±10		µA
		V_{IN} = 1.0V		±10		µA
Zi	Differential Impedance			100		Ω

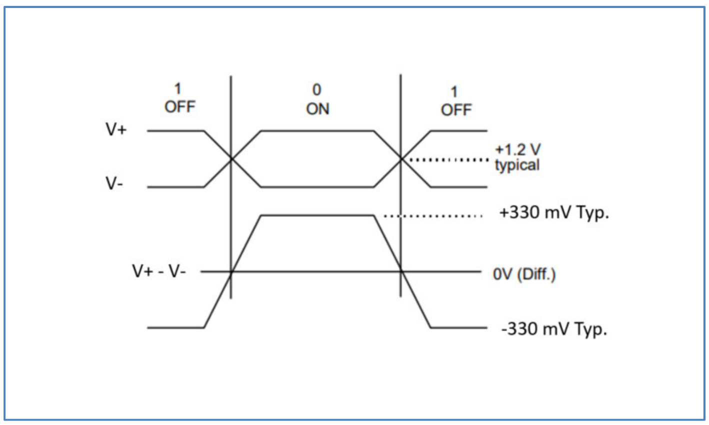


Figure 8: LVDS Levels

Table 5 LVDS AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{TCLK}	LVDS Clock Frequency	SXGA FR=60Hz		273	400	MHz
TT_{TCLK}	LVDS Clock Transition Time	F = 400MHz			0.68	ns
DC_{TCLK}	LVDS Clock Duty Cycle	F = 400MHz	45		55	%
SKWMG	Receiver Skew Margin with Deskew	F = 400MHz	200			ps

6.1.2 Video Input Timing Diagram

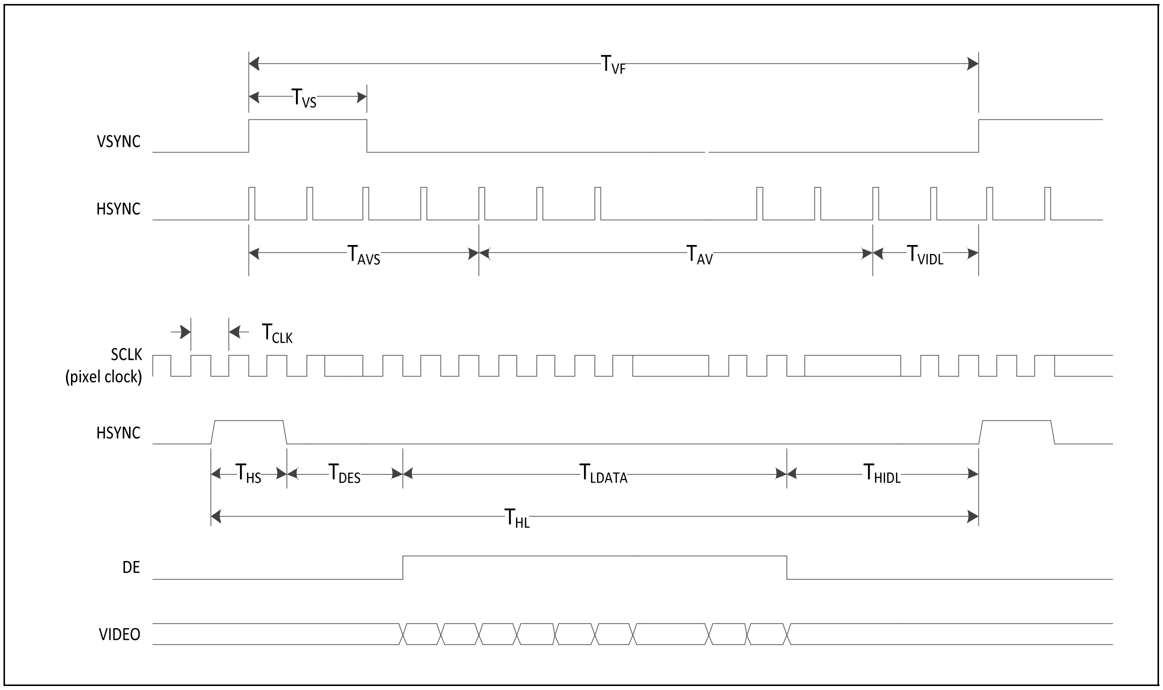


Figure 9: Video Input Timing Diagram

Table 6-6 : Video Input Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	F_{CLK}		91[1]	120	MHz
Clock Period	T_{CLK}		10.98		ns
Clock Duty	D_{CLK}	45		55	%
VSYNC Pulse Width	T_{VS}	2			HSYNC period
Time to Active Video Start	T_{AVS}	5			HSYNC period
Time to Next Vsync	T_{VIDL}	2			HSYNC period
Active Video Lines	T_{AV}	526	1024	1036	HSYNC period
HSYNC Pulse Width	T_{HS}	8			SCLK period
Time to DE Start	T_{DES}	12			SCLK period
Time to Next Hsync	T_{HIDL}	12			SCLK period
Active Video Pixel	T_{LDATA}	782	1280	1292	SCLK period
Line Overscan	T_{HL}	1200			SCLK period

Note 1: SXGA @ 60 0Hz frame rate, Reduced Blanking Mode

6.1.3 Gamma Sensor Timing Diagram

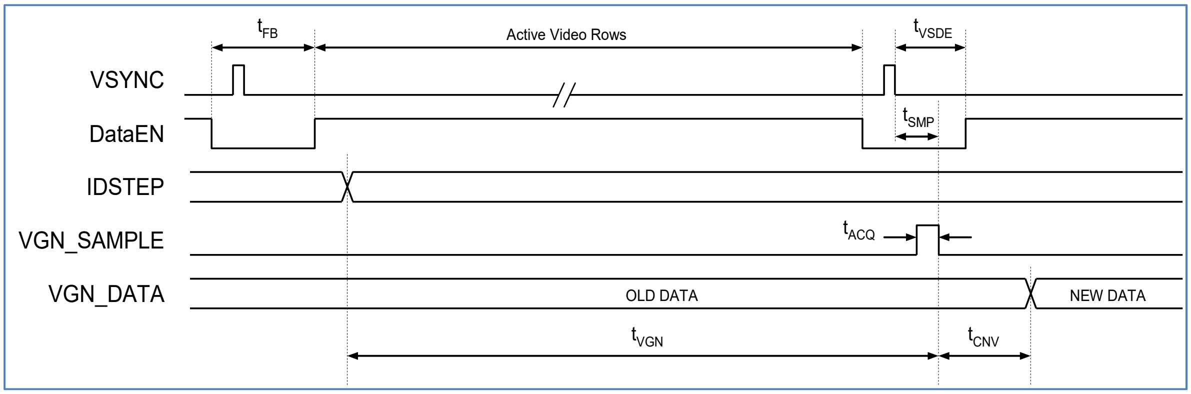


Figure 10: Gamma Sensor Timing Diagram

Table 6-7 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	1			%
VGN Sampling Time	t_{SMP}	t_{ACQ}		t_{VSDE}	
A/D Acquisition Time	t_{ACQ}	20			µs
A/D Conversion Time	t_{CNV}				

7. OPTICAL CHARACTERISTICS

7.1 Room Temperature Characteristics

Table 7-1 : SXGA-096 XLS WHITE Microdisplay Optical Characteristics
Conditions: Ta = +20ºC, VDD1.8 = +1.8V, VDD5 = +5V, VPG = -1.5V, Refresh rate: 60 Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
LPEAK	Front Luminance @ max gray level, 25% pixels on		6,000(1)	>6,000(2)	cd/m^2
LMAX	Front Luminance @ max gray level, all pixels on	3,800	4,100(3)	>5,000(4)	cd/m^2
	Variability (display to display) (5)	0	3	5	%
LMIN	Minimum display luminance @ max. gray level(6)	-	0.1	0.5	cd/m^2
CR	White to Black Contrast Ratio	1,000:1	10,000:1	> 50,000:1	
CIE White	CIE-X (1931 Standard)	0.300	0.325	0.360	
	CIE-Y (1931 Standard)	0.370	0.405	0.420	
GL	Gray Levels	-	256	256	levels
F_R	Refresh Rate	30	60	85	Hz
Fill Factor	Emissive Area/Total Sub-pixel Area		0.7		
U_{LA}	End to end large-area uniformity	75(7)	90		%
S_{VH}	Pixel spatial noise at ½ luminance (8) (1STD)			5	%
T_{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: At the center of a 800 x 800 all pixels on box

Note 2: At the center of a 800 x 800 all pixels on box. Operation at this extreme level will lead to rapid luminance degradation.

Note 3: When using on-board eeprom values to set IDRF for the targeted luminance (See 10.4)

Note 4: Assumes maximum practical IDRF/DIMCTL register values

Note 5: At gray level 255 and 1,500 cd/m2 luminance. Luminance uniformity measured between the nominal values of 9 ~500-pixel zones located uniformly over the display area.

Note 6: Spatial noise is measured at half the nominal luminance (~750 cd/m^2) and gray level 255. The measurement is the ratio of the variability (standard deviation) by the mean luminance.

7.2 Characteristics over full operational temperature range (-46°C to +71°C)

Figure 11 below shows the luminance regulation over the full operational temperature range with the display operated with 100% of pixels turned on at gray level 255 and a room temperature luminance set to ~ 4000 cd/m^2.
The typical variability (defined as (Max-Min)/(Max+Min)) is 15%

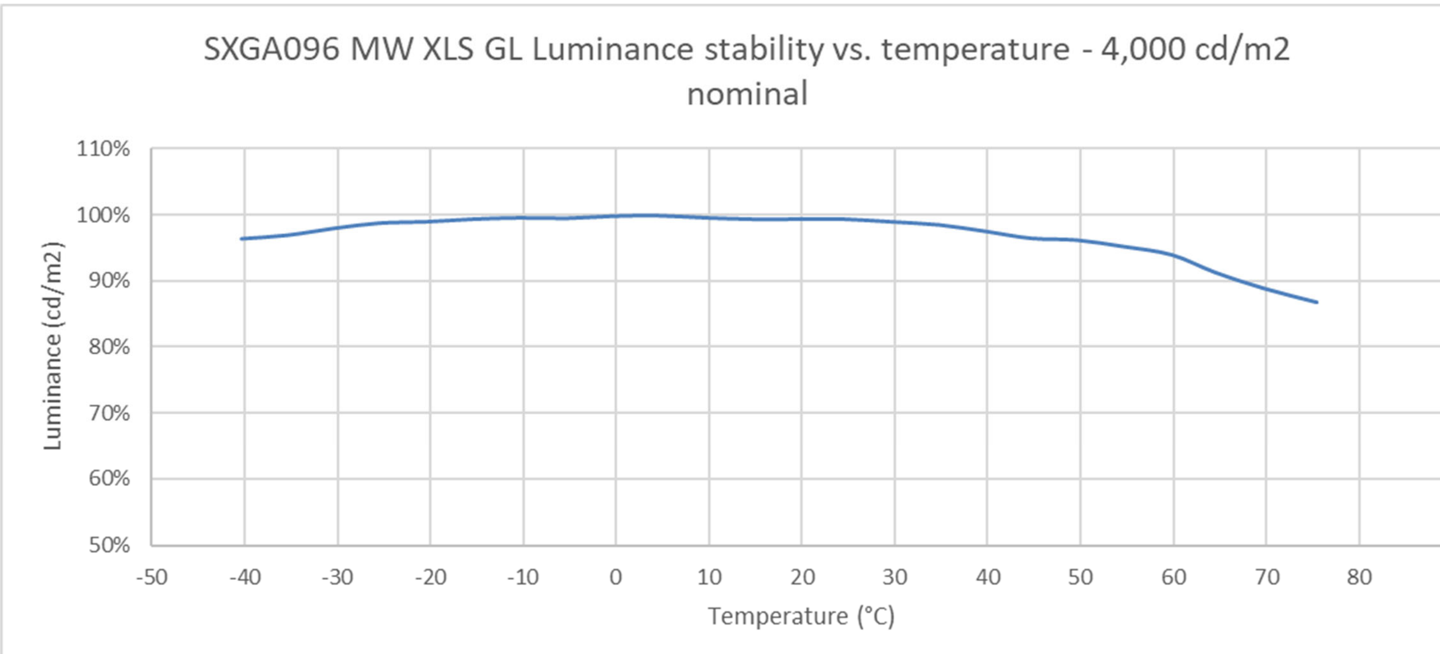


Figure 11: Luminance stability vs. Temperature

8. MECHANICAL CHARACTERISTICS

Connectors J1

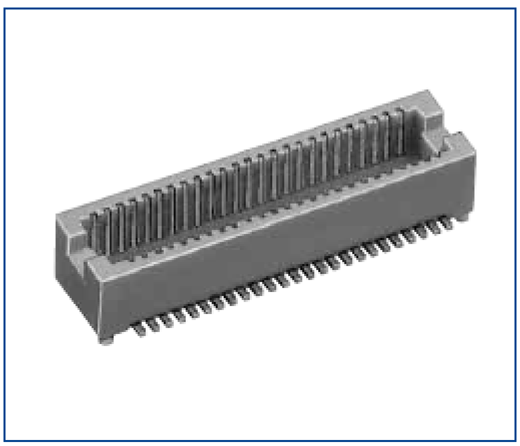
Manufacturer:	Hirose
Manufacturer Part Number:	DF12NB(3.0)-30DP-0.5V(51)

Mating Connector Information

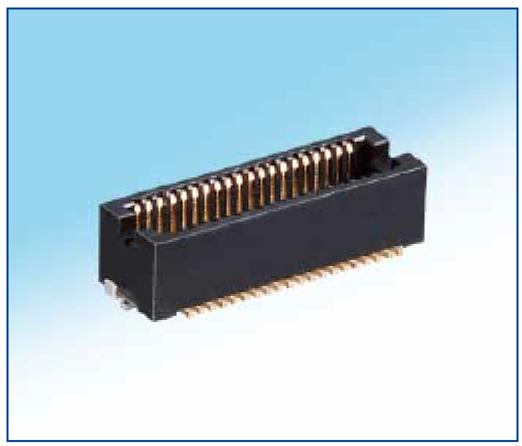
Manufacturer:	Hirose
Manufacturer Part Number:	DF12NB(3.0)-30DS-0.5V(51)

Weight:	< 3 grams
Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.25 mm (both axes)

Note
DF12D(3.0)-30DP-0.5V has been obsoleted by the manufacturer.
The replacement connector implementation started in January 2022.
The replacement connector WHITE is black, and is form/fit/function compatible with the older part number.



Older version



Current version

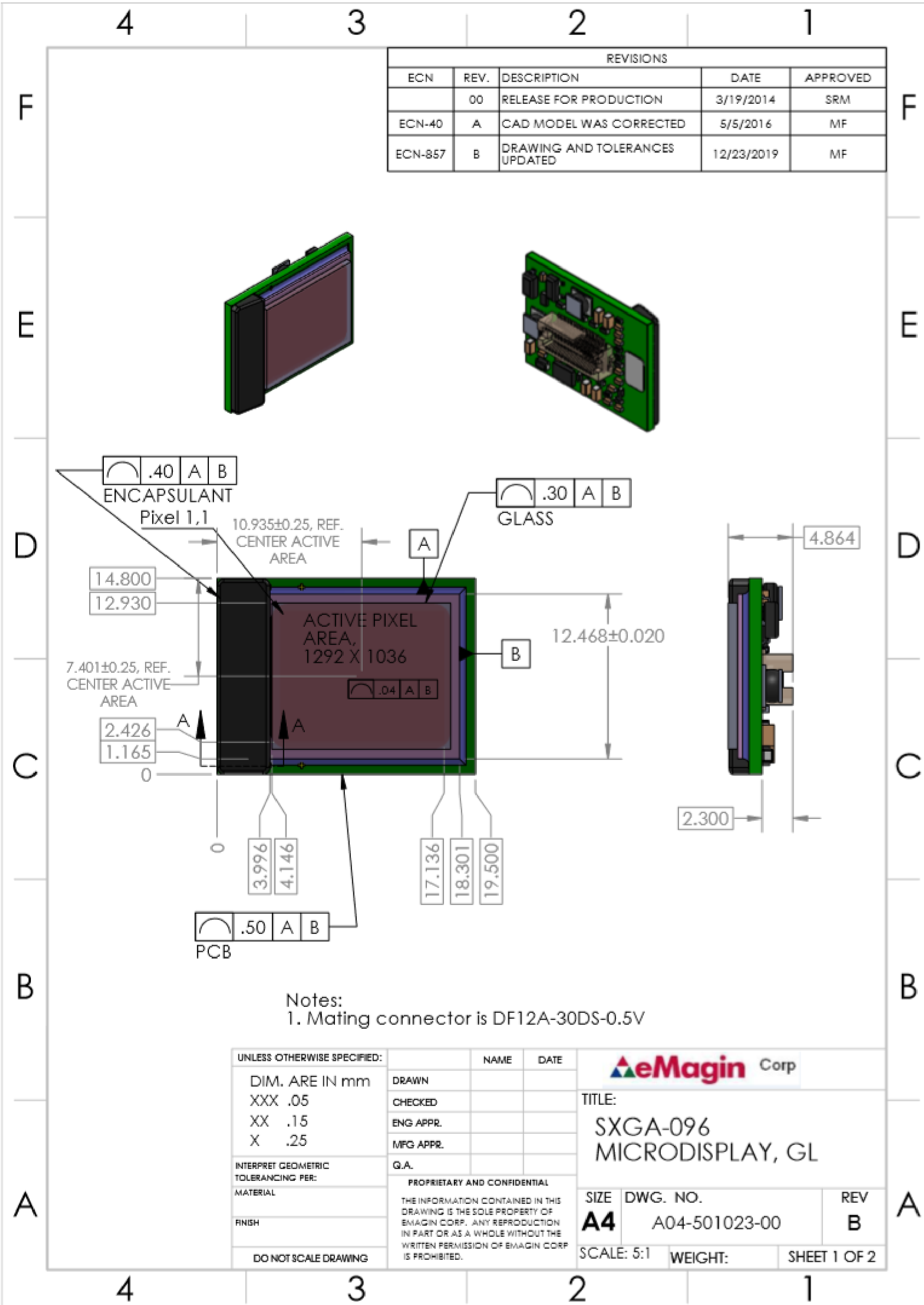


Figure 12: SXGA-096 Microdisplay Assembly

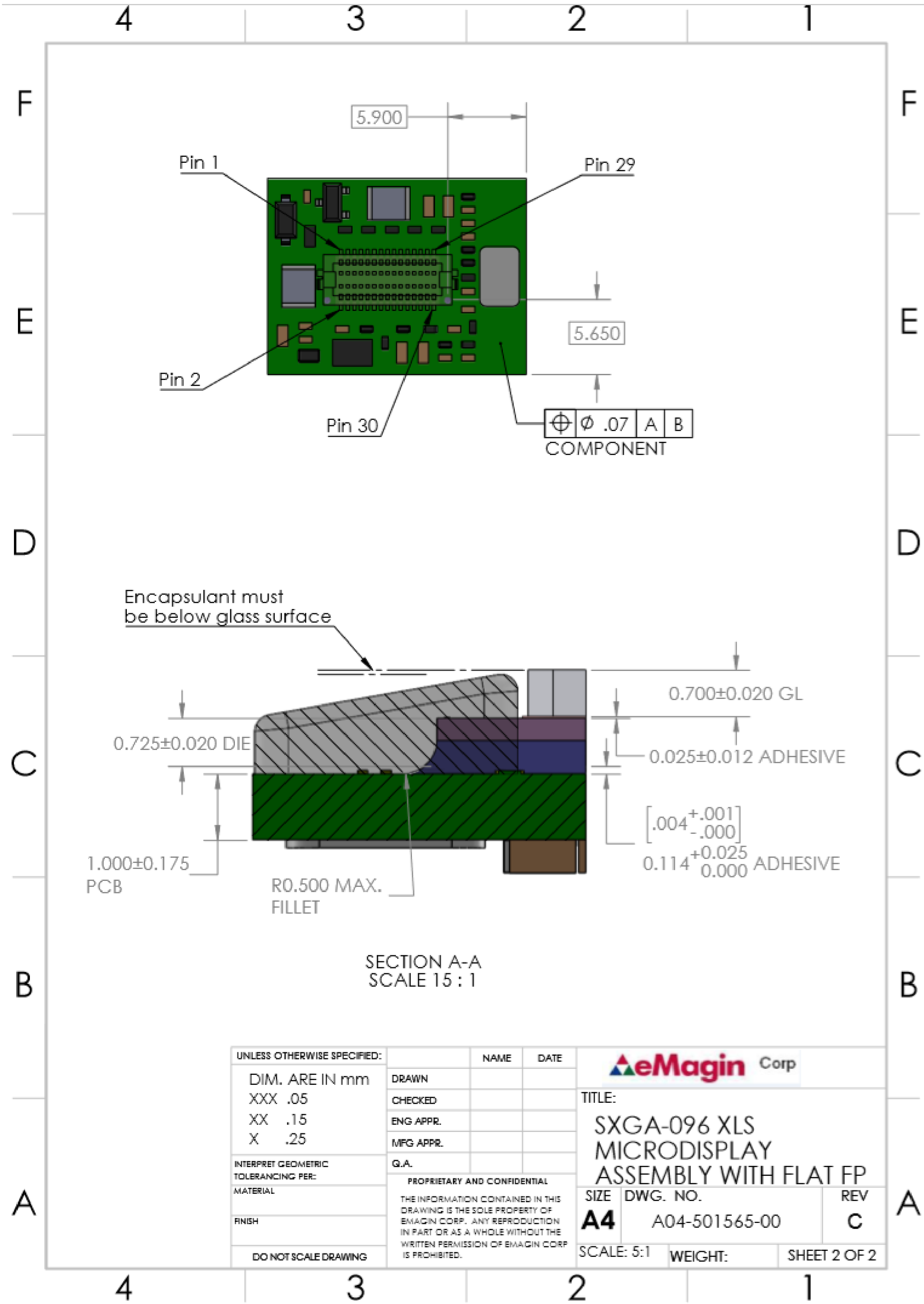


Figure 13: SXGA-096 Microdisplay Assembly - Detail

9. CARRIER BOARD SCHEMATIC

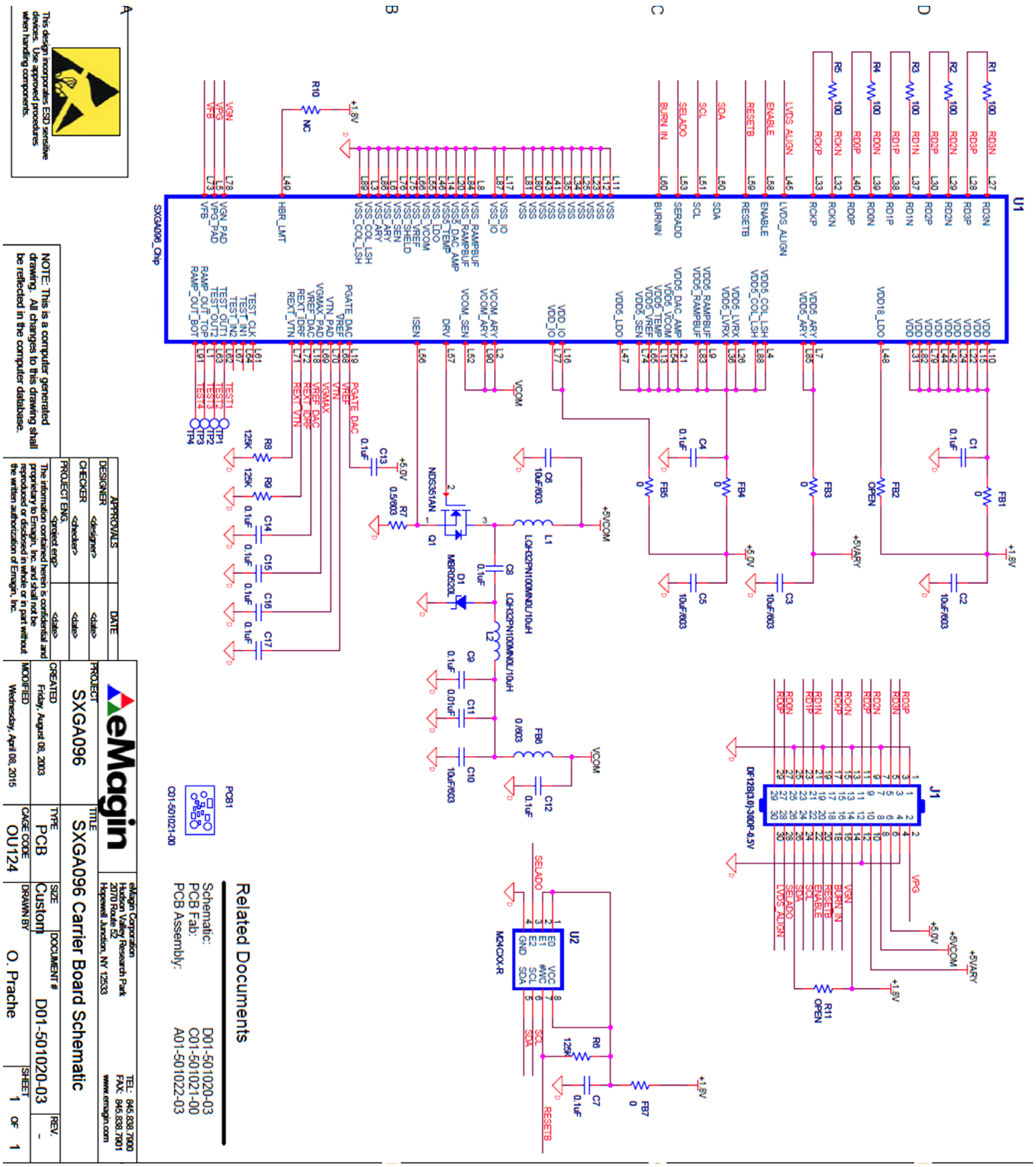


Figure 14 SXGA096 Carrier Board Schematic

10. DETAILED FUNCTIONAL DESCRIPTION

10.1 Data and Timing Interface

The SXGA096 Microdisplay physical data/timing interface uses Low Voltage Differential Signaling. The host system must format and encode the signal input according to a defined timing protocol in order for the microdisplay LVDS decoder to operate properly.
The LVDS receiver assumes an 8-bit serialization of the incoming data.
The LVDS receiver is compliant with the TIA-644A standard, except for the maximum signaling rate which cannot exceed 800 Mbps in the SXGA096 Microdisplay, assuming dual clock-edge use.

10.1.1 LVDS Receiver Overview

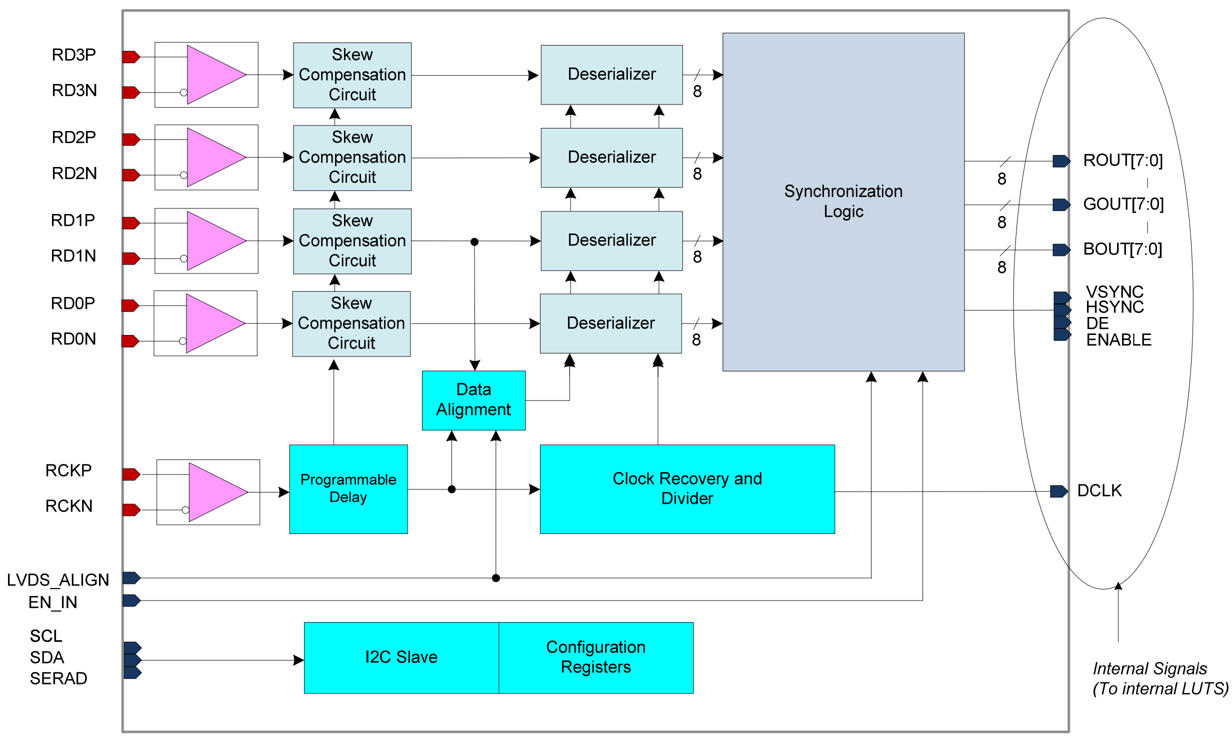


Figure 15: LVDS Receiver Block Diagram

The video interface signals are composed of 4 data pairs and one clock pair, which are the low voltage differential signaling (LVDS), and one control signal (LVDS_ALIGN), which is a CMOS signal. The receiver input pads expect an industry standard LVDS output signaling electrical characteristics. The serialization and protocol is a custom implementation that does not require a PLL circuit at the receiver end, but instead relies on a dedicated clock differential channel (RCKP/RCKN) to de-serialize the data

The LVDS data pairs must be 8-bit serialized data. The LVDS clock also should be a differential signaling pair, in the same way to the data channel with a toggle pattern. It always should be twice as fast as the pixel clock. The LVDS receiver uses both edges of clock.

Alignment of the data to the recovered clock is a two-step process, a bit alignment, followed by a byte alignment. The bit alignment is done through a skew compensation technique.
Both alignments are driven by the host system.

One consequence of this skew compensation implementation is that it can only be done at power-on, and cannot be done during normal video operation since all the LVDS channels (including the Clock channel) are used for this operation
Data alignment, on the other hand, can be done more frequently and eMagin Corporation recommends it be performed every Hsync (line) period.

10.1.2 Port Mapping

Figure 16 shows how the LVDS channels map into data (R,G,B) and control signals

Operation at a reduced power is possible by using only channels RD2 and RD3 and setting bit 6 of register 2 (DISPMODE) to 1. This is because the display is a monochrome white display where all 3 sub-pixels emit in white and can therefore have the same data value.

Bits	LVDS Data Channel			
	RD0	RD1	RD2	RD3
7	R7	G6	R0	B5
6	R1	G5	DE	B4
5	R6	G1	HSYNC	B3
4	R5	G0	ENABLE	B1
3	R4	G4	VSYNC	B0
2	R3	G3	B7	B2
1	R2	G2	G7	B6
0	VDMY1*	VDMY2*	VDMY3*	VDMY4*

* : Dummy bits for line balance

Figure 16: LVDS Data Map

10.1.3 Skew Compensation and Alignment

Figure 17 below shows the microdisplay initialization with the addition of skew compensation:

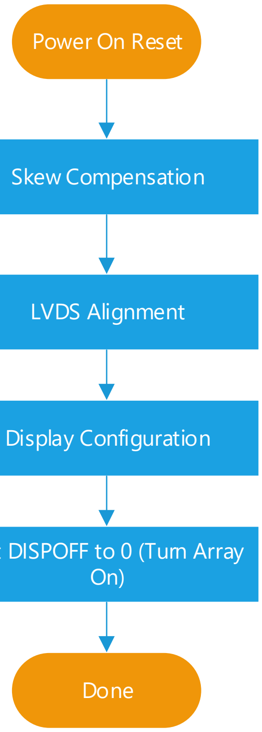


Figure 17 Initialization with optional Skew Compensation

In this mode, the paths identified below in Figure 18 are used. Delays are used for both data and clock. The DINx (where x = 0, 1, 2, 3) are captured in the SKFAST and SKSLOW registers (address 0x29, 0x2B)

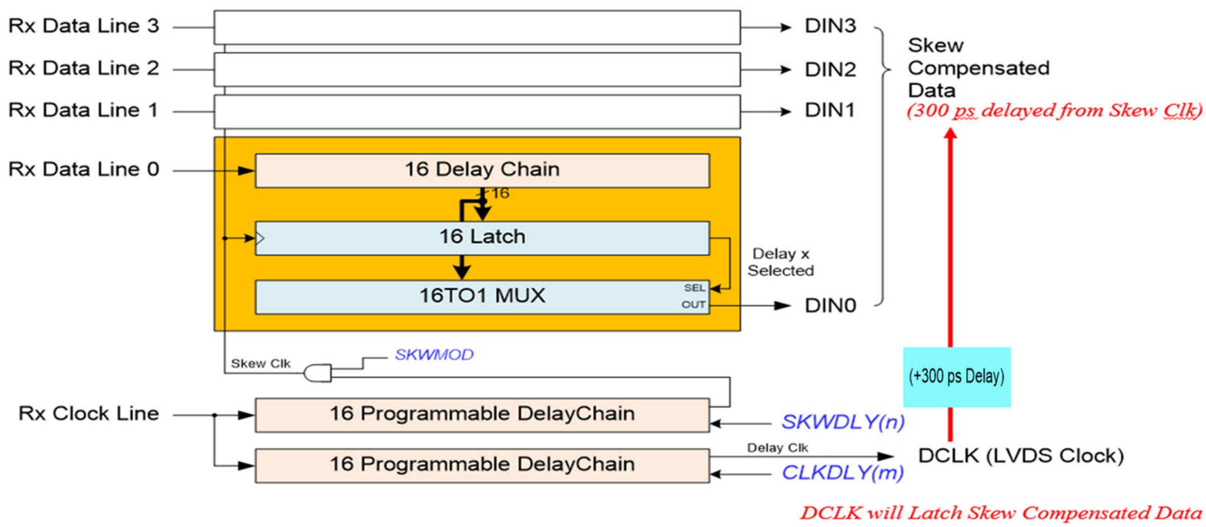


Figure 18 LVDS Alignment: Skew Compensation

Each data pair is fed through a delay chain containing 16 individual delays. The outputs of the delay chain are clocked into the SKEWn latches (n = 0 to 3). The clock is a delayed receiver clock (LVDS clock). The delay is programmable and set by the SKWDLY bits (Bits 4 to 7) of register DLYSEL (address 0x1F). Bits 1 and 16 of the SKEWn latch are written to the SKSLOW and SKFAST registers.
There are four data channels, so there are 4 bits for SKSLOW and 4 bits for SKFAST.
In addition the four 16-bit SKEW registers (SKEW0 to SKEW3) can be read and written as well (used in the Manual skew compensation mode).

The SKEWMOD parameter (bits 0 and 1 of register LVDSCTL (address 0x20) allow the user to select between 4 modes:

- Normal operation (no skew compensation action).
- Automatic skew compensation (the preferred option when using skew compensation)
- Manual skew compensation where all channels have identical SKEW registers (user sets SKEW0)
- Manual skew compensation with individual control of each channel's SKEW 16-bit register.

This document will only describe the automated skew compensation method, as the manual techniques are not recommended due to their implementation complexity.

Automatic Skew Compensation

The LVDS receiver expects a dedicated skew compensation patterns on all LVDS channels including the clock channel when power is applied and the alignment patterns to identify the MSB of the 8-bit serial data at every VSYNC at least.
The transmitter transmits 0 skew, but skew occurs at the receiver side depending on the PCB and cable transmission line characteristics. The incoming data with skew can be aligned internally by Skew Compensation.

Register SYNCMOD (Address 0x2B) needs to kept to its power-on reset value (0x02) for this phase.
Register LVDSCTL (Address 0x20) needs to be set to 0x01 for this phase.

The user starts with the minimum delay value and checks the results by reading the register SKWFAST and SKWSLOW values. The delay value (SKWDLY) is increased until SKWFAST = 0 and SKWSLOW = F. At that point, alignment is achieved. Increasing the SKWDLY further can provide a range of delays that meet the 0x0F condition, and this can be used to select an optimum value for SKWDLY (in between the minimum and maximum values that result in SKFAST = 0x0F and SKSLOW = 0x00)

At that point, the data pairs are aligned and the SKEWMOD bit can be turned off, locking the delays for each data line (Equivalent to setting LVDSCTL to 0x00).

The Data Clock (shown as DCLK in Figure 18) now needs to be delayed from the incoming Rx Clock by the same delay as SKDLY. This is done by setting CKDLY = SKWDLY.

Figure 19 below shows the basic timing for 2 of the 4 channels (for clarity)

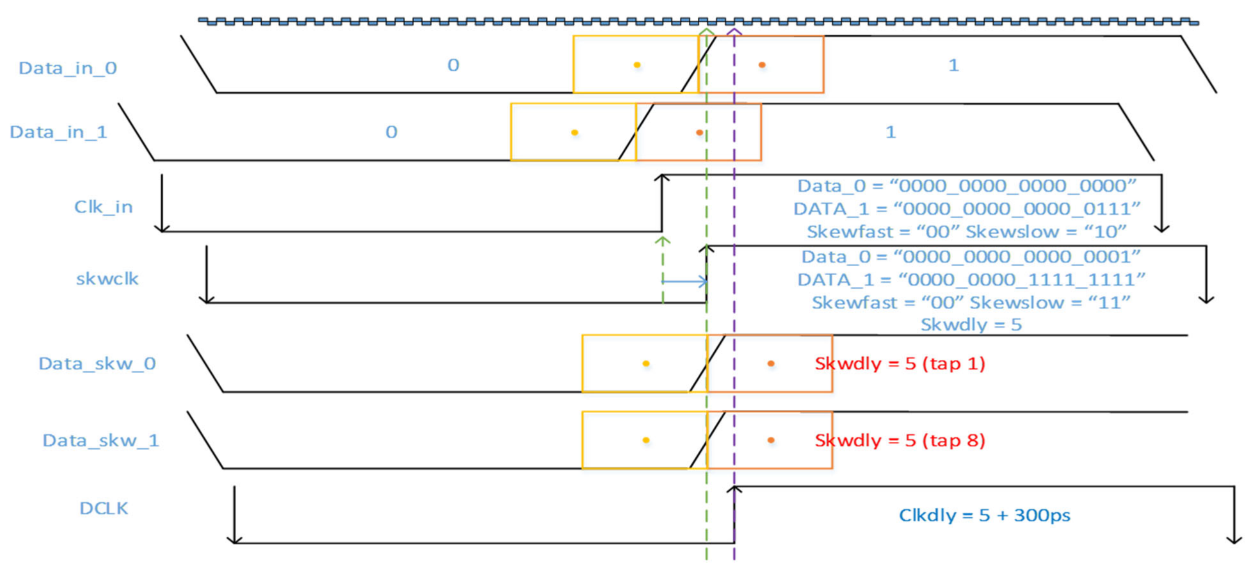


Figure 19: Basic operation concept of Skew Compensation

Skew Compensation flows:

1. Send the same "00001111" to all LVDS lines including clocks
2. Set "skew Compensation Mode" by writing I^2C register SKEWMOD to 0x1
3. Write I^2C register SKWDLY to 0 and read CHKSKW register and check if it is equal to 0xF. Otherwise, increase the value of SKWDLY register by 1 and repeat until SKFAST = 0x0F and SKSLOW = 0x00
4. If SKFAST and SKSLOW have the targeted values, then all data line has been set to the unit delay position of SKWDLY. Now write CLKDLY with the same value as SKWDLY.
5. Exit "Skew Compensation Mode" by writing I^2C register LVDSCTL to 0x0
6. All the clock and data lines back to normal video data.
7. Do the Data Alignment procedure

10.1.4 Word Alignment

After bit alignment has been completed, a word alignment step is required. The term word is used to define the 8-bit data (8-bit serialization mode).
The host outputs a dedicated pattern to the Data Channel 1, as described below, for a minimum time period, and raises the LVDS_ALIGN input shortly after. Channels 0, 2 and 3 are not used for the word alignment and their contents do not matter.
The alignment process is automatic when the ALNMOD bit (bit 2 of register LVDSCTL) is set to 1. This is the expected typical configuration where the FPGA outputs the LVDS_ALIGN signal every horizontal period. Figure 20 shows the word alignment process flow, entirely driven from the host.

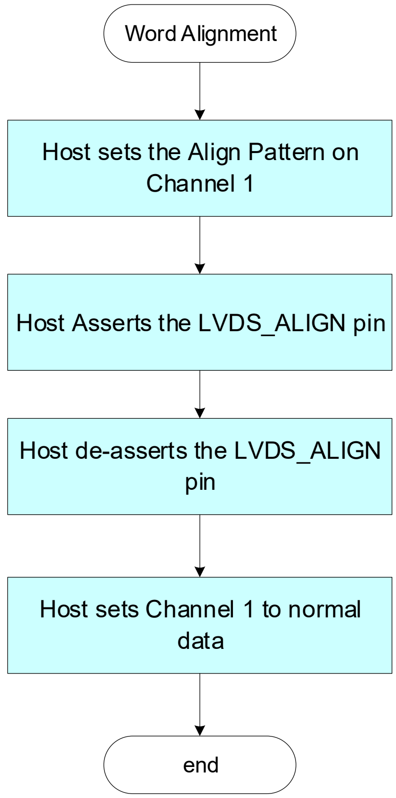


Figure 20 LVDS Word Alignment Flow Chart

Figure 20 shows how the channel 1 data pattern is constructed for the word alignment. Only bit #7 is asserted, all other bits are set to 0.
The new data pattern needs to be asserted for a minimum of two pixel clock (VCLK, source video clock in the host system) prior to asserting LVDS_ALIGN
The new data pattern must be active for at least four words before the host can de-assert the LVDS_ALIGN pin on the SXGA096 backplane.
The new data pattern must be active for at least two words after LVDS_ALIGN is de-asserted

The word alignment can be run every line during the horizontal blanking (DE_IN low state, where DE_IN is the source system Data Enable signal).

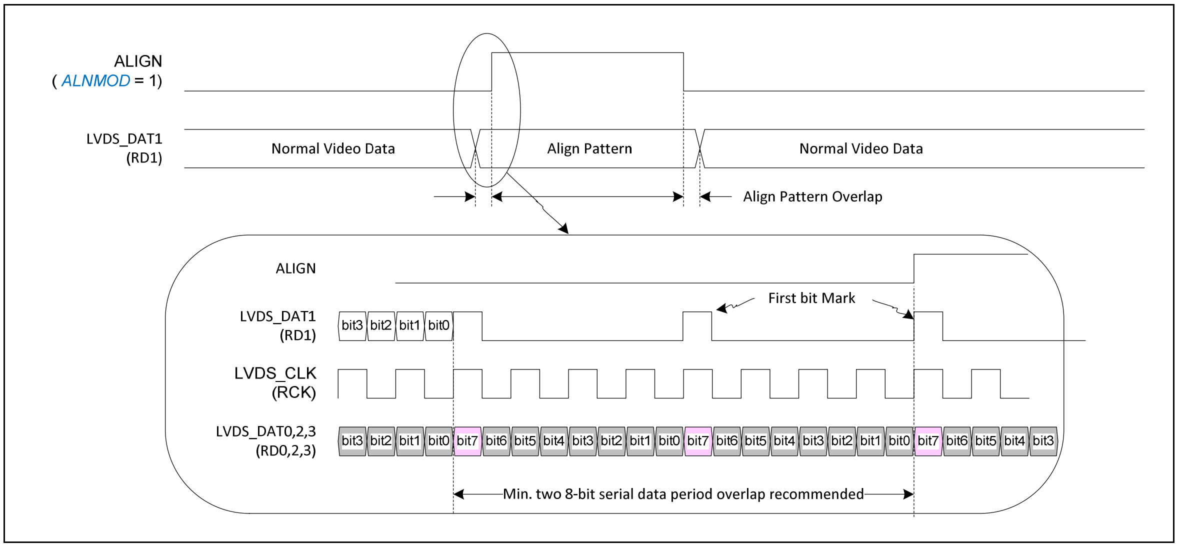


Figure 21 LVDS Word Alignment - Data Pattern

If bit ALNMOD is set to 0, there is no alignment being performed even if the FPGA sets the LVDS_ALIGN input to the microdisplay and sends the alignment pattern.
eMagin Corporation recommends the ALNMOD bit be set to 1 after the skew compensation phase to ensure optimal data integrity during normal operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CM}	Common Mode Input Range		1.0		1.8	V
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	V_{IN} = 1.8V			±10	µA
		V_{IN} = 1.0V			±10	µA
F_{TCLK}	LVDS Clock Frequency	SXGA FR=60Hz		364	400	MHz
TT_{TCLK}	LVDS Clock Transition Time	F = 400MHz			0.68	ns
DC_{TCLK}	LVDS Clock Duty Cycle	F = 400MHz	45		55	%
SKWMG	Receiver Skew Margin with Deskew	F = 400MHz	200			ps

Table 10-2: LVDS Characteristics

10.2 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

A block diagram of one column drive circuit is shown in Figure 22. The 1292 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

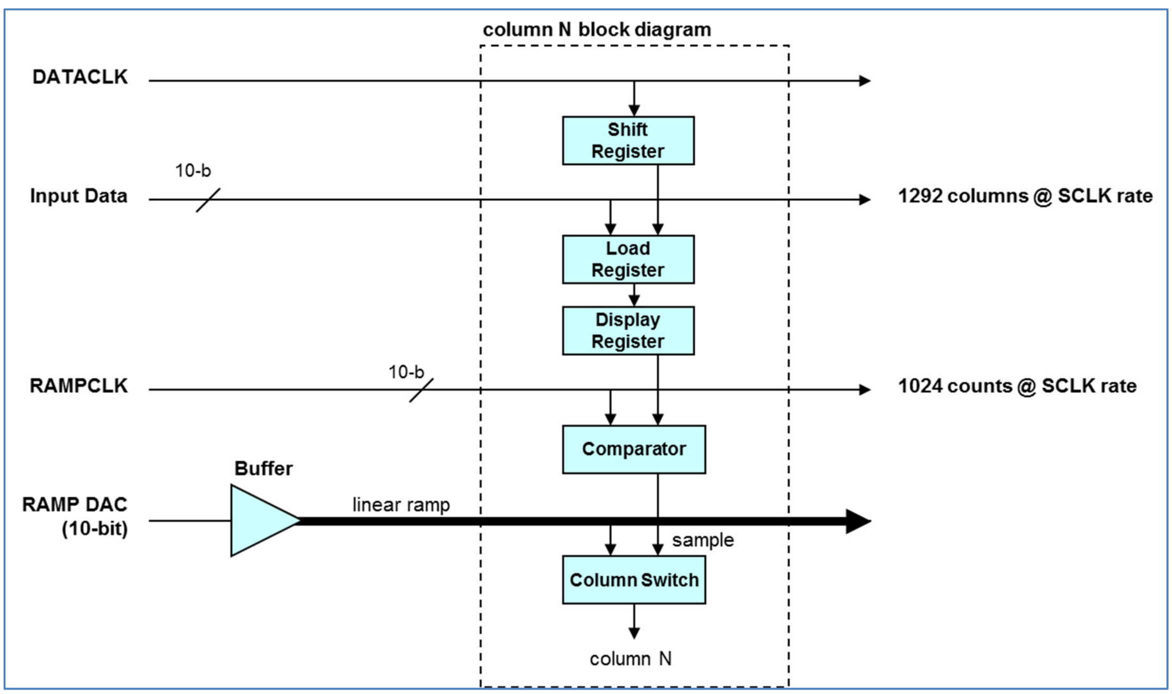


Figure 22: Data sampling for Column N

A timing diagram for the data sampling process is shown in Figure 23 . The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VDD5 rail after 1024 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via register bits RAMPDLY, its peak value can be set using register VDACMX, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

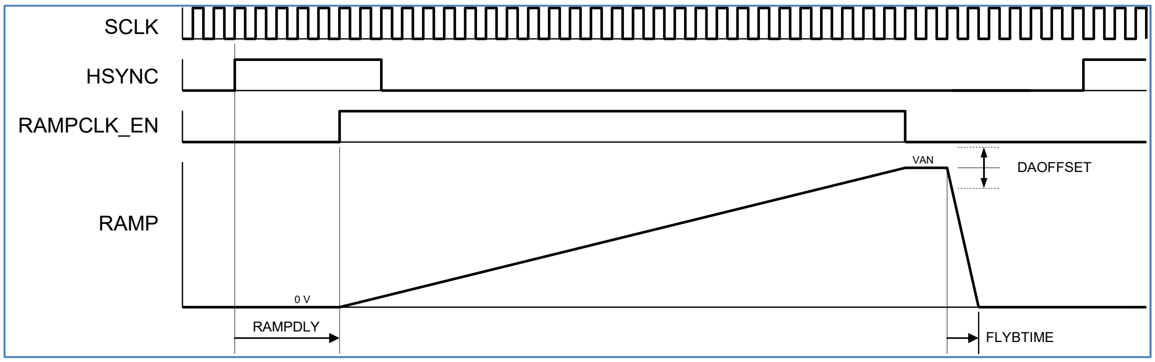


Figure 23: Timing diagram for column data sampling

10.3 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, LFTPOS, RGTPOS, TOPPOS and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before a video image is displayed.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

10.3.1 Vertical Position Control

To support the vertical positioning of the display within the extra 12 pixels provided on each column of the array, an on-chip shift register function is provided in the Row sequencer logic, and controlled by registers TOPPOS and BOTPOS. The starting row for the active video is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in SXGA mode is vertically centered in the array. The Vertical positioning logic will blank rows at the beginning and end of each frame of data to allow a vertical image shift of up to 12 pixels in steps of 1 or 2 pixels in SXGA mode.

10.3.2 Horizontal Position Control

To support the horizontal positioning of the display within the extra 12 pixel provided on each row of the array, an on-chip shift register function is provided after the LUT block, and controlled by registers LFTPOS and RGTPOS. The Horizontal Shifter adds black pixel data to the beginning and end of each line of data to allow a horizontal image shift of up to 12 pixels in steps of 1 pixel in SXGA mode.

10.3.3 Interlaced Modes

Bits SCMODE in the DISPMODE register are used to select either progressive (default) or interlaced modes.

Field status in interlaced mode is provided via the ENABLE input pin. The state of this pin is latched on the falling edge of VSYNC. When register bit SET_FIELD = "0" then a logic low at the ENABLE pin indicates that Field 1 (odd field) is active, and a logic high indicates that Field 2 (even field) is active. The opposite states are indicated when SET_FIELD is set to 1.

10.3.4 Stereovision Mode

The SXGA-096 is designed with binocular stereovision applications in mind. As a result of the fast OLED response time and the presence of a storage capacitor at each pixel, it has been verified that the microdisplay can operate at low refresh rates without showing flicker.

This allows the displays to be used with a frame or field sequential (more generally known as time sequential) stereovision mode using a single video input channel, and therefore providing a simple means to leverage the capabilities of PC compatible computers using stereo compatible graphics adapters, such as the NVidia GeForce series. The frame sequential stereovision mode supported should follow the Video Electronics Standards Association (VESA) Connector and Signal Standards for Stereoscopic Display Hardware. This standard is available from VESA at www.vesa.org.

The ENABLE input pin allows for a direct implementation of the VESA standard without additional external components. The microdisplay can be programmed for either an active high or low Enable, allowing a single signal to be used with two displays. In such a configuration, one display scans and displays while the other one holds and displays.

The ENABLE input acts, when set low, as a mask for HSYNC and VSYNC. It does not blank the display but prevents it from acquiring another frame of data until released. This is a real time input. The active state (high or low logic level) is programmed by the SET_ENABLE bit in the VINMODE resister.

The 3D-MODE bit of the DISPMODE register will be used to set either Time Sequential mode to activate the stereovision mode of operation (1) or Normal (non-3D) operation (0).

Frame Sequential Mode:
In Time Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE=”1” the SCMODE bits in the DISPMODE register are set to Progressive Scan Mode (00H) for frame sequential mode. The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard mentioned above, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The stereovision mode is controlled by both the Enable input pin and by the SET_ENABLE bit of the VINMODE register. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= “0”). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display must be configured with Enable active high (SET_ENABLE=”1”). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

Field Sequential Mode:
In Field Sequential Mode each video field in an interlaced image contains information for either the left or right eye. Consequently, the resolution is reduced in half for each display.

When 3D-MODE=”1” the SCMODE bits in the DISPMODE register are set to either Interlaced or Pseudo Interlaced Mode to activate field sequential mode. The operation of the Enable input pin and the SET_ENABLE bit will be similar to Frame Sequential Mode except that now the Enable input toggles at the field rate. The polarity of the field corresponding to the active state of the ENABLE input will be set by the SET_FIELD bit in the VINMODE register. When SET_FIELD=”0” the odd field is applied during the active state for ENABLE, and the even field is assumed during the active state for ENABLE when SET_FIELD=”1”.

For standard WVGA operation, the SET_ENABLE bit needs to be set to 0 (logic low), which is the power-on default value, and the Enable pin input needs to be tied to Ground.

10.4 Luminance Control

When VCOMMODE = 0x00 (Automatic Vcom mode), the microdisplay luminance is controlled by two registers, IDRF and DIMCTL. IDRF is used to set the maximum brightness while DIMCTL is used to modulate the percentage of the maximum brightness from 0 to 128% of the value set by IDRF. An internal sensor provides automatic luminance regulation over temperature (±10% from nominal at 20°C).

When VCOMMODE = 0x02, the microdisplay luminance is controlled by the VCOM register. In this mode, called manual Vcom mode, there is no luminance regulation over temperature and the control range is limited to 256 levels. This mode was included as part of the original design but is not recommended for typical operational use.

The VCOMMODE = 0x01 setting is not recommended for typical use.

10.4.1 Automatic Mode Luminance Control (Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is implemented by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRF. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRF_COARSE in register IDRF provide a coarse adjustment of the maximum luminance level, while the IDRF_FINE bits enable the coarse level to be fine-tuned. **Error! Reference source not found.** shows the typical luminance output at gray level = 255 in a WHITE display for various settings of the IDRF and DIMCTL registers.

The IDRF functional block design results in duplicate luminance settings: IDRF values (hexadecimal) from 0x10 to 0x1F will produce the same brightness as IDRF values from 0x20 to 0x2F. Refer to **Error! Reference source not found.** for a graphical representation of Luminance as a function of IDRF.

The maximum useable value of IDRF is 0xDF, beyond which the value will roll over to 0x00 and increment again (for example writing 0xE8 is equivalent to writing 0x08).

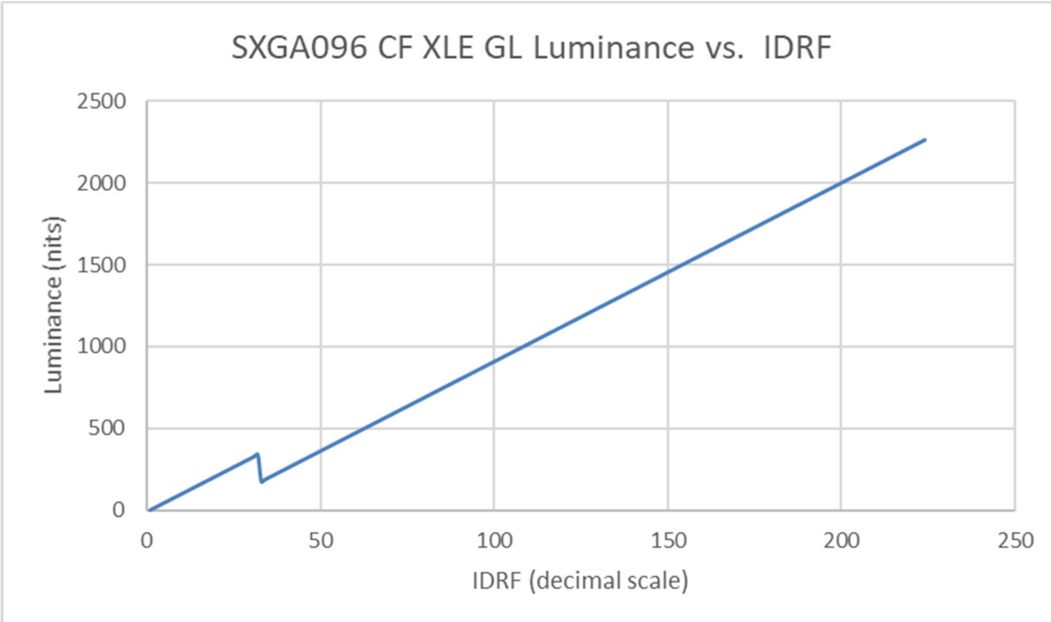


Figure 24: luminance profile for various IDRF settings

While the maximum luminance shown in Figure 19 exceeds 2,200 cd/m2, eMagin Corporation recommends keeping the level to no more than 5,000 cd/m2 in order to ensure adequate useful life.

The 7-bit DIMCTL register modulates the luminance set by the IDRF value from ~0% to 128%. It is therefore possible to control the display luminance by using DIMCTL alone, once the maximum luminance has been set by the IDRF register.

While the overall behavior shows a linear response, for lower values of IDRF and DIMCTL, the response changes.

Register range limitations

The microdisplay luminance is set by the product of the IDRF register value times that of the DIMCTL register divided by 100:

$$L \alpha \text{ IDRF x DIMCTL /100}$$

However, it is not practical to use the full range of either the IDRF or DIMCTL registers:

- Maximizing these registers will lead to a luminance level that exceeds the recommended maximum, and will lead to an accelerated luminance degradation over time. eMagin Corporation records for each microdisplay the IDRF setting for reaching 4,100 nits with all pixels on, and saves this value to the on-board eeprom at address 0x22 (See Appendix

15 for eeprom map details). A higher luminance can be readily achieved at the same setting with fewer pixels turned on (refer to Table 7-1, LPEAK parameter).

- Minimizing these registers will result in loss of linearity followed by a lack of control (no change) of luminance below a certain value that varies from display to display. At room temperature, the product IDRF x DIMTCL/100 (decimal values), should not go below 10 to preserve control. This will be roughly equivalent to a 250-300 cd.m^{-2} luminance. Lower levels can be reached by using the PWM mode, described below in section 10.4.2.

The minimum useable value for IDRF is 0x08 (with DIMCTL =0x7F)
The minimum useable value for DIMTCL is 0x08 (with IDRF = 0x80)

A luminance lower than 250-300 cd.m^{-2} is also possible by adjusting the data value (0 to 255), but at the expense of dynamic range.

10.4.1.1 Luminance Setting

The SXGA-096 microdisplay luminance can be set to an absolute value using information included in the on-board eeprom at addresses 0x8E to 0x91.
The luminance is a linear function of IDRF for values of IDRF greater than 32 (decimal code).) that can be expressed as:

L = slope x IDRF (decimal) – intercept (decimal)

The information in registers 0x8E (142d) to 0x90 (144d) provides the slope and intercept values that govern the Luminance vs. IDRF linear equation.
Register 0x8E provides the integer part of the slope (High-Slope, see 10.4.1.2)
Register 0x8F provides the fractional part of the slope
Registers 0x90 and 0x91 provide the origin (High-Origin) value (Theoretical luminance value for IDRF = 0. It is theoretical because the linear equation is only valid for IDRF >20h (32 decimal)). Values for High-Origin range from 0 to 65535.

Register 0x90 is the high-byte register
Register 0x91 is the low-byte register

The slope and intercept values are calibrated for each display as part of the manufacturing process. With these values, the calculated luminance is in cd/m^2 units (nits).
The accuracy of the calculated value is smaller than or equal to 3% for a luminance up to 900 cd/m^2, and better than 5% beyond 900 cd/m^2.

This allows precise matching between displays when used in a binocular application, as well as exceptional consistency of performance from display to display.

10.4.1.2 DC-DC Converter configuration vs. target luminance

The DC-DC converter that generates the negative common voltage VCOM, described in section 10.5, is controlled by the VCOMCTL register (Address 0x0F), and adjustments are needed based on the targeted microdisplay luminance.
For brightness levels below 2,000 $cd.m^{-2}$ (without use of the PWM functionality), VCOMCTL should be set to 0x0D.
For brightness levels above 2,000 $cd.m^{-2}$, VCOMCTL should be set to 0x29

At the same IDRF setting, changing the VCOMCTL value will result in a luminance change of about 6-7%, which may be undesirable in some applications. In order to compensate for this offset, the method described below can be used:
Luminance is roughly linear with respect to IDRF and that is true regardless of the VCOMCTL value. Therefore the luminance vs. IDRF behavior can be modeled by a linear equation and, when ready to change the VCOMCTL value, two simple equations using only IDRF and values

stored in the microdisplay on-board eeprom, are enough to adjust the IDRF value to maintain the same luminance within 1-1.5%.

The values for the slope and origin of the Luminance vs IDRF linear equation when VCOMCTL = 0x0D are measured during factory acceptance test and saved in the eeprom at addresses 0x92 to 0x95. They will be referred to as Low-Slope and Low-Origin

Register 0x92 provides the integer part of the Low-Slope
Register 0x93 provides the fractional part of the Low-Slope
Registers 0x94 and 0x95 provide the Low-Origin value (integer number 0 to 65535)

10.4.1.3 Dimming range extension using PWM

As seen above, using only IDRF and DIMCTL registers will limit the minimum achievable luminance (all pixels on) to about 60-70 cd.m^{-2}
For applications requiring a lower luminance level, it is necessary to make use of the ROWRESET registers which control the pulse-width modulation (PWM) mode.

10.4.2 Row Duty Rate Control

The duty rate for a row of data is defined as the fraction of a frame period during which the pixels maintain a programmed value; for the remainder of the frame period the pixels will be driven to black.

A Row Reset function is provided in the SXGA096 to allow the duty rate of rows to be controlled between 0 and 100% (default condition). The register ROWRESET[9,0] is used to set the number of Hsync cycles during which the pixel data is driven to black during a frame period. For ROWRESET=0 the pixel data is never driven to black and the duty rate for pixel data is equal to 100% (default). For ROWRESET=W the pixels in any row are driven to black for the final 2*W Hsync cycles in an active frame period.

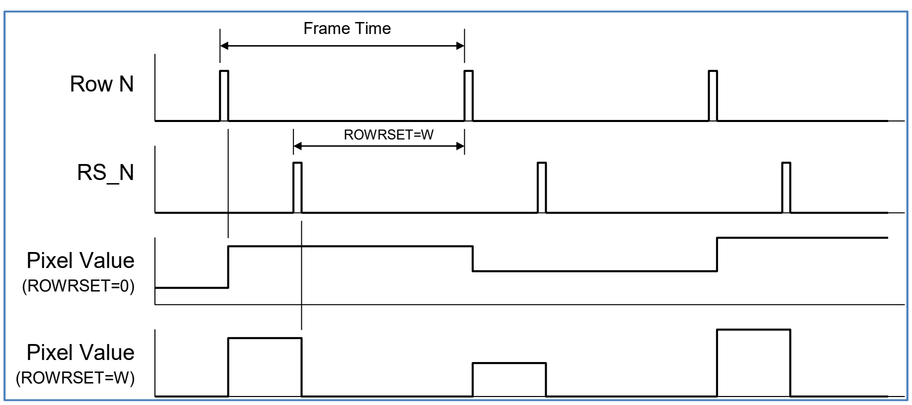


Figure 25 : Timing diagram showing Row Reset functionality.

The operation of the Row Reset function is depicted in the timing diagram shown in Figure 25. All the pixels contained in ROW N are programmed during the Nth horizontal line scan following the initialization line scans which occur at the beginning of a video frame. Normally this pixel data is stored in the pixel and remains unchanged until it is refreshed during the next frame period. When the Row Reset function is activated, the pulse RS_N is generated at a position determined by the value of register ROWRESET. For example, when the register value is equal to W the rising edge of RS_N occurs exactly 2*W Hsync cycles after the programming cycle for ROW N. The pulse RS_N sets all the pixels in ROW N to black until the next programming cycle. All rows in the array will operate at the same duty rate. As a result the duty rate for all the rows in the pixel array will be given by

$$ROW\_DUTY = \frac{2 * W * T_{HSYNC}}{T_{FRAME}}$$

This function can be used to control dimming (see section 9.4.5) to extend the display dimming range. A side benefit of this function, when used for dimming, is that no gamma update is needed when dimming is done exclusively with the Row Reset function.

Another use of this function is to reduce motion artifacts: the net visual effect of limiting the on-time of a given row is a reduction in visual persistence. This allows the eye to "forget" the state of the row prior to its update with potentially new information, and leads to the perception of a smoother motion when an object in the image changes position from frame to frame.
The exact value of the Row Reset registers for this function are application dependent and the user must determine what constitutes an acceptable configuration.

10.4.3 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a gamma-corrected optical response from the SXGA-096 display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The SXGA-096 display gamma sensor generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage output which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value $\boldsymbol{VGN_i}$., corresponding to one of 8 internally fixed grayscale levels $\boldsymbol{GL_i}$, is selected by setting bit IDSTEP in register GAMMASET via the serial port. The IDSTEP values correspond to luminance levels in a power of 2 sequence where IDSTEP = 0x7 corresponds to full scale (equivalent to graylevel equal to 256, and IDSTEP = 0x0 corresponds to minimum scale (equivalent to gray level 2) (Refer to Table 3). The VGN signal is internally fixed for a full-scale output range of VDD5/2. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word $\boldsymbol{DVGN_i[9,0]}$ using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

where $\boldsymbol{VGN_{MAX}}$ is VDD5/2. Each of these data values must be further multiplied by a correction factor $\boldsymbol{CF_i}$ to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

where empirically determined values for factor $\boldsymbol{CF_i}$ are given in Table 9

Table 9: SXGA096 CF XLS Correction Factors

CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.914	0.959	0.947	0.951	0.960	0.966	0.979	1

Using the derived values for $\boldsymbol{GC_i}$ and their corresponding grayscale coordinates $\boldsymbol{GL_i}$, the 8-entry Gamma Correction table consisting of data points $\boldsymbol{Q_i} = (\boldsymbol{GL_i}, \boldsymbol{GC_i})$ can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 10-5, for a white luminance ~1,000 cd/m^2.

Table 3: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
IDSTEP[0]	0h	1h	2h	3h	4h	5h	6h	7h
$\boldsymbol{VGN_i}$ ***(volt)***	1.590	1.648	1.681	1.710	1.794	1.852	1.977	2.155
$\boldsymbol{GC_i}$ ***(dec)***	689	750	755	772	817	848	918	1023
$\boldsymbol{GL_i}$ ***(dec)***	2	4	8	16	32	64	128	255

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in 7. The input to the LUT for each WHITE of the video source is represented by the 8-bit signal VIN[7,0], and the output of the LUT (which is also the input to the microdisplay) is represented by the 10-bit signal DIN[9,0]. For example, the Y coordinate for the intermediate point Q(x, y) on the line segment formed between the gamma table points Q6 and Q7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations before loading it into the data-path LUTs in the microdisplay. A buffer LUT is used in the microdisplay to temporarily store the data as it is transferred from the microcontroller via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

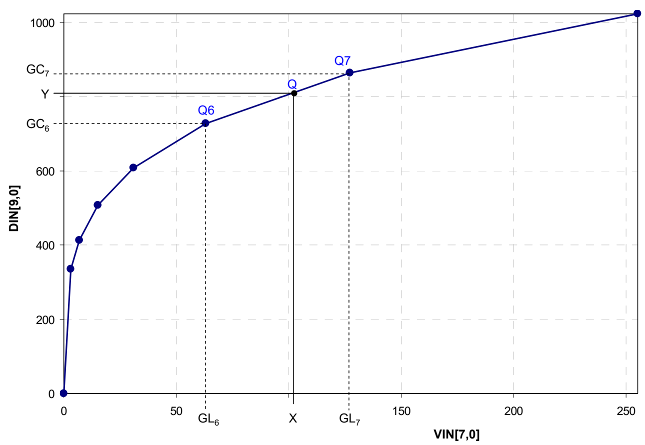


Figure 26 : Generating intermediate points by linear interpolation

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 26 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the SXGA-096 design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

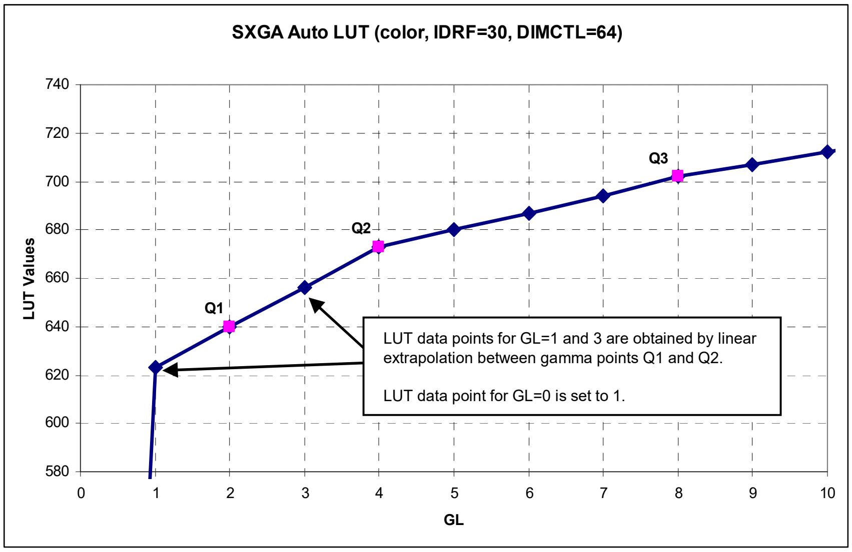


Figure 27 : Gamma curve at low gray levels

Figure 28 and Figure 29 show a typical gray scale response for a Gamma = 1 at different luminance values (1,500 cd/m^2 and 150 cd/m^2)

Figure 28: Typical Luminance Gamma Response

Figure 29: Low Luminance Gamma Response

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^{\gamma}$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^{\gamma} = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^{\gamma} * 1023$$

For the case of a linear optical response (γ=1) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the

System Gamma parameter are shown in Figure 30 and the corresponding system response curves for the display are given in Figure 31.

The System Gamma function is implemented in DRK Firmware and is accessible to the user in the DRK GUI Software .

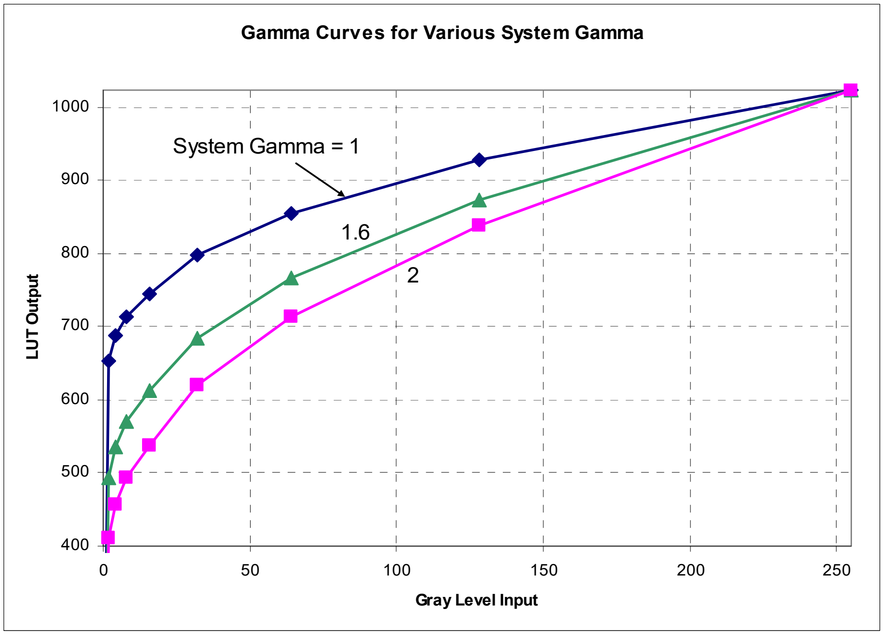


Figure 30 : Gamma curves for arbitrary System Gamma

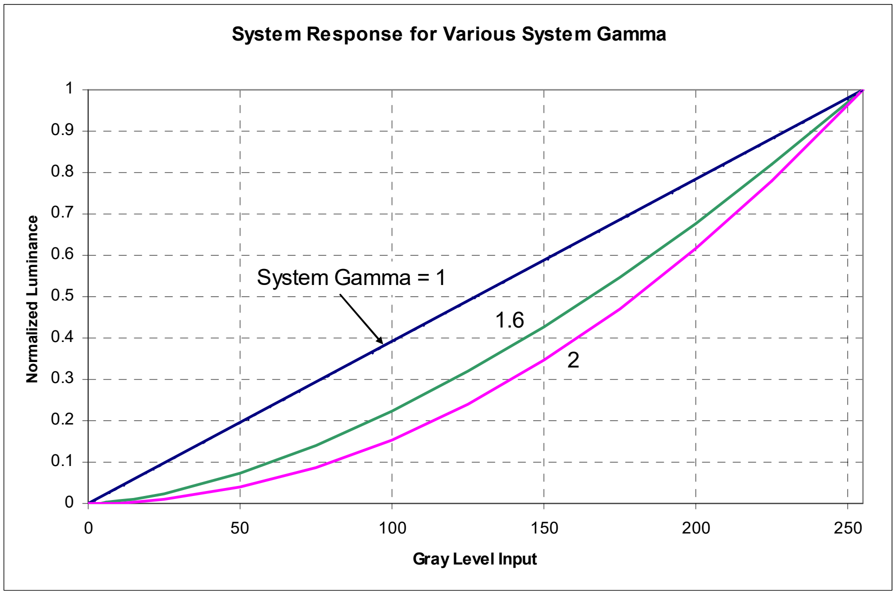


Figure 31 : Display system response for arbitrary system gamma

10.4.4 Temperature Readout

Description

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register ANGPWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (16H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

Register TEMPOFF is calibrated at Factory Acceptance Test with register TREFDIV = 0x17. This value has been optimized for the -60°C to +80°C range.
With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(°C) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60ºC will return a TEMPOUT reading of 0 and temperatures above +80ºC will return a hexadecimal value of FF.

Calibration

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX}, the expected sensor response would be as follows:

$$TEMPOUT\ (dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$

$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60ºC to +80ºC are given by the following values:

TREFDIV = 0x17 and TEMPOFF = 0x75

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum value for TEMPOFF which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=23d=17h , TUPDATE = 0x10, and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0ºC, 20ºC, 40ºC, 60ºC
- Take the slope to find the sensor response, A_{MEAS} = dTEMPOUT(d)/dtemp
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=23d=17h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read $TEMPOUT_{AMB}$ and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - TEMPOUT_{AMB}$$

10.5 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VDD5 to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0], VCOMCTL[7,0] and VCOMMODE[3,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A block level schematic of the Cuk converter that is employed in the SXGA-096 application is shown in Figure 32.

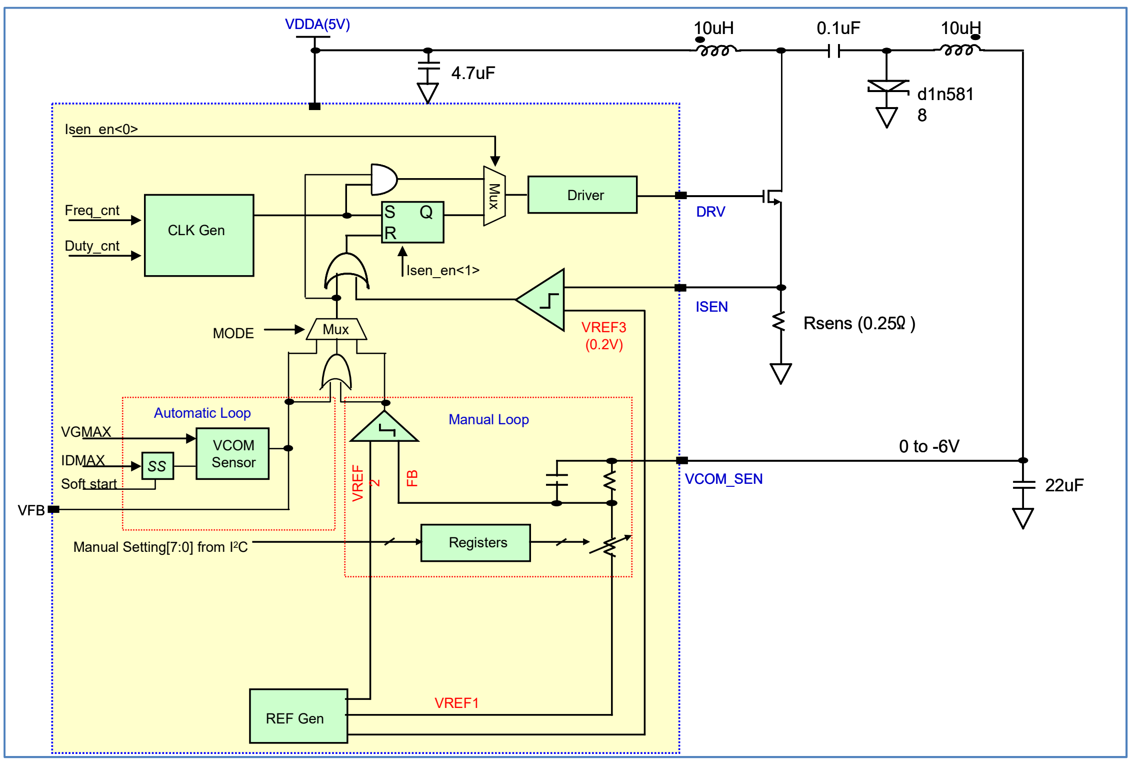


Figure 32 : Schematic of DC-DC controller function

Three modes of operation, selected via register VCOMMODE, are provided for the controller function. Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=1h, is not recommended for typical operation.

Mode 3, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the brightness control via IDRF and DIMCTL is not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.
In addition, there is no luminance regulation over temperature when using this mode.
For applications with limited temperature range and low precision for brightness setting, the Mode 3 provides for a single register control.

10.6 Serial Interface

10.6.1 Serial Port Controller Overview

The serial interface consists of a serial controller and registers. The serial controller follows the I2C protocol. The serial controller is capable of slave mode only.
There is no on-board pull-up resistor on the SDA line. It is the host system responsibility to provide the SDA pull-up termination resistor.

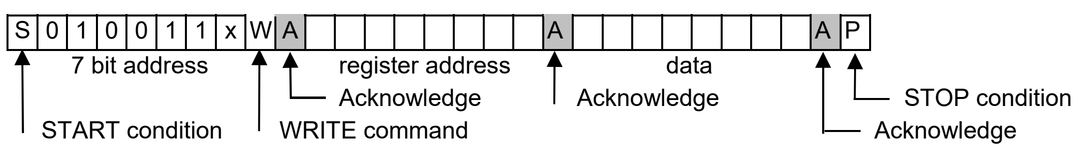
An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

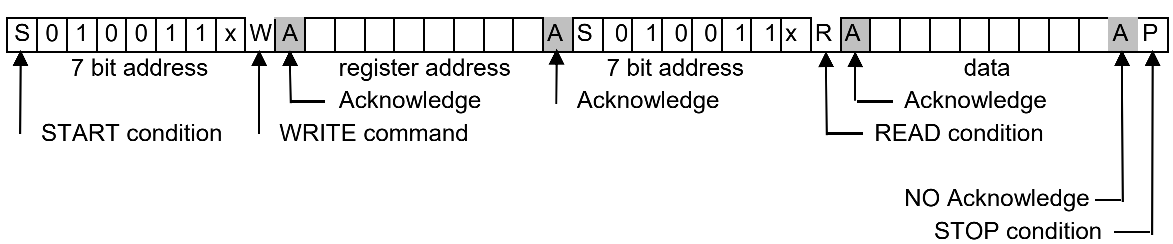
The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010011X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 10-5.

Write Mode: Address is 4C (or 4E if SERADD = 1)

Read Mode: Address is 4D (or 4F is SERADD =1)

Sequential Read/Write Operation

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

It is possible to run the I^2C interface without source clock or any sync signals. The I2C interface operates independently of the LVDS interface.

10.6.2 On-board I2C Devices

There are two I2C compliant slave devices in the SXGA096 Microdisplay assembly

- The SXGA096 Microdisplay backplane
- The on-board EEPROM

The Microdisplay backplane serial address is as follows:

Write Mode: Address is 4C (4E)

Read Mode: Address is 4D (4F)

The EEPROM serial address is as follows:

Write Mode: Address is A6h

Read Mode: Address is A7h

Interface maximum frequency: 400 KHz.

Table 10-6 : I2C Address Summary

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Address (Hex)
							SA	R/W	
Write	0	1	0	0	1	1	0	0	4C
Read	0	1	0	0	1	1	0	1	4D
Write	0	1	0	0	1	1	1	0	4E
Read	0	1	0	0	1	1	1	1	4F

10.7 Power-On Sequence

To ensure proper startup and stabilization of the display the following power-on sequence is recommended:

1. Turn on VDD1.8, VDD5 and VPG supplies (these can be simultaneous)
2. A ramp-up time of 0.2 to 20ms for VDD5 and VDD1.8 is recommended for best performance
3. The ramp-up time for VPG is not critical and it can be turned on anytime
4. Configure the display registers to the desired startup state
5. Turn on the display by setting the DISPOFF bit in register DISPMODE to "0"

Figure 33 shows the timing diagram for the power supplies and control signals during startup when the display is first turned on. The external supply voltages (VDD5, VDD1.8, and VPG) can all be applied at the same time as in the diagram. An internal power-on-reset signal is triggered when both the VDD5 and VDD1.8 voltages exceed a built-in threshold level. After a delay of about 70ms the internal dc-dc controller is activated which generates a negative supply for the common cathode of the array. The video display is enabled 20ms later and video is displayed on the array after the DISPOFF bit has been set to "0" via the serial port. Prior to this moment the pixels in the array are actively driven to the black state. The pin RESETB must also be logic high before any registers can be written.

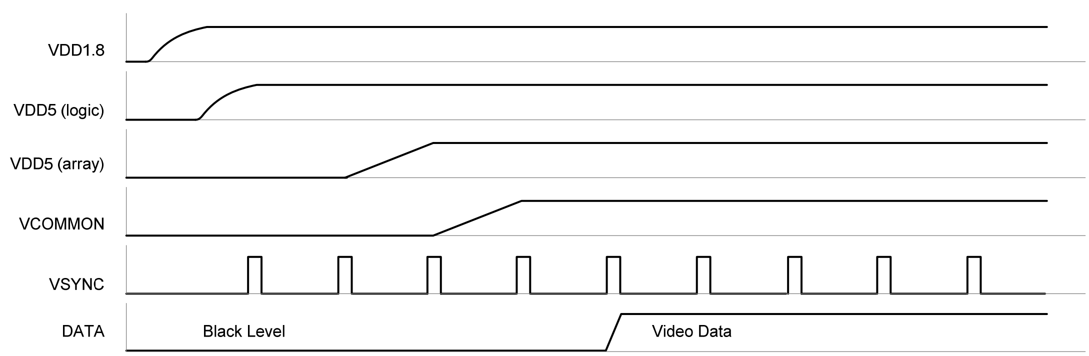


Figure 33 : Power-Up sequence for supplies and control.

During the power down operation, the supply rails should be switched off in the reverse order to the power up sequence. When the POR function detects a drop in the VDD1.8 supply below a minimum operating threshold it will immediately switch off the Row and Column sequencing circuits. At the same time the VCOMMON supply will be turned off followed by the 5V array supply. The power-down sequence is illustrated in Figure 34.

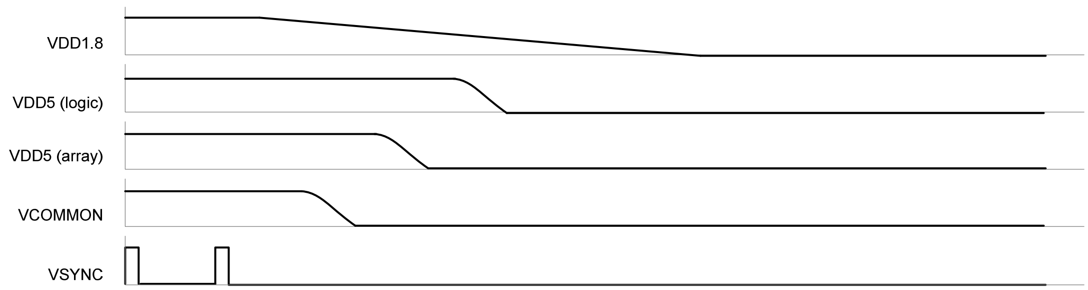


Figure 34 : Power-Down sequence for supplies and control.

10.7.1 Display Off Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the black state until the DISPOFF bit (bit 7) in register DISPMODE is set to 0. The DISPOFF bit, when set to 1, will force all pixels to the off (black) state.
.

10.8 Power Savings Modes

The circuit shall provide power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register SYSPWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control - many functional blocks have the option to be turned off individually via control of registers ANGPWRDN and SYSPWRDN.

10.9 Built-In Test Patterns

The IC includes functionality to simplify the external hardware requirements for test of OLED microdisplays and applications. The display is self-powered for this mode with no external video, sync, or clock signals required. The display starts in this mode with a simple, flat white field at maximum luminance by default and without the need for register setting.

The BI mode is activated at start-up when a dedicated pin TMODE is set to logic level 1 or PATTEN bit in register TPMODE is set high. The internal dc-dc converter oscillator is used to generate the basic timing sequence (VSYNC, HSYNC, and SCLK). The vertical frequency will be set to 60Hz.

The microdisplay luminance is adjusted by two dedicated registers (IDRF-BN, DIMCTL-BN) when the display is configured to use the internal test pattern generator. These registers mirror the IDRF and DIMCTL register with respect to functionality and are located at the following addresses:

IDRF-BN at 0x41
DIMCTL-BN at 0x42

By default an all-pixels-on pattern will be displayed. The following extra test patterns are included and are accessed via the serial interface:

000 = all white pattern (default)
001 = WHITE bars
010 = gray scale (without gamma correction)
011 = checkerboard pattern
100 = alternating columns pattern
101 = alternating rows pattern
110 = grid pattern
101 = all black
111 = WHITE screen based on TPWHITE register value.

Use with registers TPLINWTH, TPCOLSP, TPROWSP and TPWHITE to modify the patterns according to **Error! Reference source not found.**.

Test Pattern Name	PATTSEL (1BH:2-0)	TPLINWTH (1CH)	TPCOLSP (1DH)	TPROWSP (1EH)	TPWHITE (1FH)	
					(1FH:2-0)	(1FH:6-4)
All White	000	X	X	X	X	X
WHITE Bar	001	X	X	X	X	X
Gray Scale	010	X	X	X	X	X
Checker Board	011	X	X	X	111	000
Alternating Column	100	LW	CS	X	111	000
Alternating Row	101	LW	X	RS	111	000
Grid Pattern	110	LW	CS	RS	111	000
All Black	101	X	X	X	000	000
All White	101	X	X	X	111	111
All Red	101	X	X	X	100	100
All Green	101	X	X	X	010	010
All Blue	101	X	X	X	001	001
WHITE Screen	111	X	X	X	8 bit value applied to all 3 WHITE	

Figure 35 : Test Patterns

X: Don't care, LW: Line Width (0~255), CS: Column Space (0~255), RS: Row Space (0~255)

11. REGISTER MAP SUMMARY

I2C Slave Address : 0100 11x

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STAT	R	REV	2-0	0	Silicon Revision Number
01	VINMODE	R/W	WRDISABLE	7	0	I^{2}C Register Write Disable 0 = Write Enable, 1 = Write Protected (Read Only)
			Reserved	6	0	Do Not Change
			DVGA	5	0	DVGA video input mode enable 0 = SXGA video mode, 1 = DVGA video mode
			SET_ENABLE	4	0	ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high
			SET_FIELD	3	0	FIELD Polarity 0 = Odd Field when ENABLE=Active, 1 = Even Field when ENABLE=Active
			AUTOSYNC	2	1	Auto HSYNC/VSYNC polarity detection enable (Detected polarity overrid VSYNCPOL/HSYNCPOL) 0 = Disable , 1 = Enable
			VSYNCPOL	1	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			HSYNCPOL	0	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
02	DISPMODE	R/W	DISPOFF	7	1	Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off
			MONO	6	0	Mono display mode 0 = Color display mode, 1 = Mono display mode (Green video input data used as mono video)
			GAMMA_EN	5	1	Internal Gamma LUT Enable (BURNIN mode override to Bypass Internal Gamma) 0 = Bypass Internal Gamma LUT, 1 = use Internal Gamma LUT
			3D-MODE	4	0	3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode
			SCMODE	3-2	0	Progressive or Interlaced scan mode select 00 = Progressive, 01 = Interlaced, 1X = Pseudo Interaced
			VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
			HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
03	LFTPOS	R/W		7-0	06	Column Display Left Position
04	RGTPOS	R/W		7-0	06	Column Display Right Position
05	TOPPOS	R/W		7-0	06	Row Display Top Position
06	BOTPOS	R/W		7-0	06	Row Display Bottom Position
07	ROWRESET	R/W		7-0	0	Row Duty Control 0:Disable, Each line displayed ROWRESET*2 Line period
08				9-8		
				12	0	ROWRESET work on UNENABLED frame in 3D mode
09	RAMPCTL	R/W	RAMPMON	5	0	Internal Ramp Buffer Monitor Enable
			Reserved	4	0	Do Not Change
			RAMPHIGH	3	0	Internal Ramp DAC set All High 0 = Normal operation, 1 = DAC set All High
			FLYBTIME	2	0	Ramp Fly back Time 0 = 800 nSec, 1 = 500 nSec
			RAMPDLY	1-0	1	Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK
			RAMPBCM	7-4	4	Ramp Buffer Current Control (0000 = -75%(Don't use), 0001 = -75%, 0010 = -50%,0 011 = -25%, 0100 = ±0%, 0101 = +25%, 0110 = +50%, 0111 = +75%,...), 25% increase for each step
			RAMPACM	3-0	4	Ramp Amp Current Control (0000 = -75%(Don't use), 0001 = -75%, 0010 = -50%, 0011 = -25%, 0100 = ±0%, 0101 = +25%, 0110 = +50%, 0111 = +75%,...), 25% increase for each step
0B	VDACMX	R/W		7-0	80	Ramp DAC Max Value Control, -40% ~ +40 %
0C	BIASN	R/W	EXT_VREF	3	0	External VREF Enable
			BIASN	2-0	1	000 = bias current off 001~111 = bias current set to 0.5nA, 1nA, 1.5nA, 2nA, 2.5nA, 3.0 nA, 3.5 nA
0D	GAMMASET	R/W	PMPHOLD_EN	4	0	VCOM PUMP hold enable when VGN sampling time 0 = Normal pumping, 1 = Pump hold function enable
			VGNSH_EN	3	0	VGN Sample & Hold Enable 0 = VGN SH Bypass, 1 = Enable VGN SH output
			IDSTEP	2-0	0	Current level for gamma sensor
0E	VCOMMODE	R/W	ISEN_EN	3-2	1	VCOM I-Sensor Enable
			VCOMAUTO	1-0	0	00 = AUTO1 mode 01 = AUTO2 mode 10 = MANUAL mode

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
0F	VCOMCTL	R/W	SS_BYPASS	7	0	VCOM Soft Start Bypass mode 0 = Soft Start function enable, 1 = Soft Start Bypass
			VCKDUTY	6-4	3	VCOM Clock Duty Control (High:Low) 0=1:7, 1=1:3, 2=3:5, 3=1:1, 4=5:3, 5=3:1, 6=7:1, 7=Don't use
			VCKSEL	3-2	3	VCOM Clock Select 0=125KHz, 1=250KHz, 2=500KHz, 3=800KHz
			VCOMSS	1-0	1	VCOM Soft Start Delay Time Mode 0 = 2mS, 1 = 4mS, 2 = 8mS, 3 = 16mS
10	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
11	VCOM	R/W		7-0	51	VCOM manual setting (used when VCOMMODE = 01 or 10 , default = -2.3V)
12	IDRF	R/W	IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
			IDRF_FINE	4-0	0	Fine adjustment for array reference current
13	DIMCTL	R/W		6-0	01	Dimming level control (default = 1X IDRF)
14	TREFDIV	R/W		5-0	17	Temp. Sensor Reference Clock Divider
15	TEMPOFF	R/W		7-0	3A	Temp. Sensor Offset
16	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * $PERIOD_{FRAME}$ $PERIOD_{FRAME}$ = 16.6 mSec when using 60Hz Video
17	TEMPOUT	RO		7-0	-	Temperature Sensor Readout
18	ANGPWRDN	R/W	ISENPD	7	0	ISEN Power Down
			IDMAXPD	6	0	IDMAX Power Down
			VCOMPD	5	0	VCOM Power Down
			VREFPD	4	0	VREF Power Down
			GMSENPD	3	0	Gamma Sensor Power Down
			VCSENPD	2	0	VCOM Sensor Power Down
			TSENPD	1	0	Temperature Sensor Power Down
			TREFPD	0	0	Temperature Reference Power Down
19	SYSPWRDN	R/W	PDWN	7	0	All System Power Down (Override all analog power down, except LDOPD, POR50VPD, POR18VPD)
			LVDSPD	6	0	LVDS receiver Power Down
			LDOPD	5	0	1.8V LDO Power Down
			RBUFPD	4	0	RAMP Buffer Power Down
			RAMPPD	3	0	RAMP DAC AMP Power Down
			DACPD	2	0	RAMP DAC Power Down
			POR50VPD	1	0	5V POR Power Down
			POR18VPD	0	0	1.8V POR Power Down
1A	TPMODE	R/W	TPVCLK	4	0	Enable external clock for Burn-in test mode (0=use internal ring OSC, 1=use external LVDS clock)
			PATTEN	3	0	Test Pattern Display Enable when "1"
			PATTSEL	2-0	0	Select test pattern for Built-In-Test-Mode (BURNIN pin = 'High' or PATTEN = 1) 000= Burn-in (all white), 001=Color Bar, 010=16 level gray scale 011=Checker Board, 100=Vertical Line, 101= Horizontal Line, 110=Grid Pattern, 111=Color Screen
1B	TPLINWTH	R/W		7-0	0	Line Test Pattern Line Width (0=1pixel, 1=2pixel, …, 255=256pixel)
1C	TPCOLSP	R/W		7-0	0	Line Test Pattern Column Space (0=1pixel, 1=2pixel, …., 255=256pixel)
1D	TPROWSP	R/W		7-0	0	Line Test Pattern Row Spce (0=1pixel, 1=2pixel, …, 255=256pixel)
1E	TPCOLOR	R/W		7-0	0	When PATTSEL=1,2 :Bit7-Bit0 :Don't care When PATTSEL=3,4,5,6 :Bit6-Bit4 :Line Test Pattern Background Color (RGB) Bit2-Bit0 :Line Test Pattern Background Color (RGB) When PATTSEL=7, All 8 bits used 256 gray level
1F	DLYSEL	R/W	SKWDLY	7-4	0	Select LVDS Skew Align reference Clock delay 0 = no delay, 1 = one unit delay, …. ,15 = 15 unit delay
			CLKDLY	3-0	1	Select clock delay for serial data latch 0 = no delay, 1 = one unit delay, …. ,15 = 15 unit delay

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
20	LVDSCTL	R/W	ALNMOD	2	0	LVDS Align mode 0 = normal Operation, 1 = auto align mode
			SKEWMOD	1-0	0	LVDS Skew mode 0 = normal Operation, 1 = auto skew, 2 = manual skew one set for all (use SKEW0), 3 = manual skew separate setting
21	SKEW0	R/W		7-0	0	LVDS data line #0 skew setting (when SKEWMOD=2, SKEW0 override others)
22				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
23	SKEW1	R/W		7-0	0	LVDS data line #1 skew setting
24				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
25	SKEW2	R/W		7-0	0	LVDS data line #2 skew setting
26				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
27	SKEW3	R/W		7-0	0	LVDS data line #3 skew setting
28				15-8		0000h = no delay, 0001 = 1 unit delay, ... FFFFh = 15 unit delay
29	SKFAST	R	SKFAST	3-0	-	MSB of SKEW3~SKEW0 read out All "0" = OK, Not all "0" = Error (need increase SKWDLY)
2A	SKSLOW	R	SKSLOW	3-0	-	LSB of SKEW3~SKEW0 read out All "1" = OK, Not all "1" = Error (need decrease SKWDLY)
2B	SYNCMOD	R/W	DEFEN	2-1	1	define ENABLE/VS pin function 00=not used (all embeded), 01=used as ENABLE, 10=used as VSYNC
			DEFHS	0	0	define HS/ALIGN pin function 0 = use as ALIGN function only, 1 = used as HSYNC and ALIGN function
2C	LUT_ADDR	R/W		7-0	0	Gamma Look-Up Table template access Address
2D	LUT_DATA	R/W	LUT_DATAL	7-0	0	Gamma Look-Up Table template R/W Data LSB (Auto LUT_ADDR increase)
2E			LUT_DATAH	9-8	0	Gamma Look-Up Table template R/W Data MSB
2F	LUT_UPDATE	R/W	UDGAMMA	3	0	Update LUT template ro R,G,B Gamma LUT enable (Auto cleared after update)
			UDRGB	2-0	7	Select R,G,B Gamma LUT to update (ex. 100=R Gamma Update)
30	Reserved	R		7-0	-	Test Purpose
31				10-8		
32	Reserved	R		7-0	-	Test Purpose
33				10-8		
34	Reserved	R/W		7-0	99	Do Not Change
35	Reserved	R/W		7-0	99	Do Not Change
36	Reserved	R/W		3-0	0	Do Not Change
37	Reserved	R/W		6-0	0	Do Not Change
38	Reserved	R/W		7-0	0	Do Not Change
39	Reserved	R/W		7-0	0	Do Not Change
3A	Reserved	R/W		7-0	FF	Do Not Change
3B	Reserved	R/W		7-0	0	Do Not Change
3C	Reserved	R/W		4-0	0	Do Not Change
3D	Reserved	R/W		2-0	3	Do Not Change
40	Reserved	R/W		6-0	0	Do Not Change
41	IDRF-BN	R/W		7-0	30	Do Not Change
42	DIMCTL-BN	R/W		6-0	64	Do Not Change

12. DETAILED REGISTER DESCRIPTIONS

12.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
REV	2-0	0	Silicon revision number; Rev. 1 = 0

Bits REV in this register indicate the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

12.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
WRDISABLE	7	0	I^2C register write disable
Reserved	6	0	Do Not Change
DVGA	5	0	VGA Video Input Mode Enable
SET_ENABLE	4	0	ENABLE active level
SET_FIELD	3	0	Field polarity
AUTOSYNC	2	1	Automatic VSYNC/HSYNC Polarity Detection Enable
VSYNCPOL	1	1	VSYNC polarity
HYSYNCPOL	0	1	HSYNC polarity

WRDISABLE:

1 = write protected (all other registers become read only)
0 = write enable (all registers can be updated externally via I^2C) (default)

DVGA:

0 = SXGA video mode (default)
1 = Double VGA video mode

When the video source is the VGA resolution, the SXGA-096 makes the pixel data double internally and display it in 1280 x 960 pixel area with this register enable.

SET_ENABLE:

0 = the active state of the ENABLE input is set “low” (default)
1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

The ENABLE input pin is also used to indicate field polarity in non-3D interlaced modes. In this mode the SET_FIELD bit determines the field polarity when ENABLE is active.

SET_FIELD:

0 = Odd Field when ENABLE=Active (default)
1 = Even Field when ENABLE=Active

The SET_FIELD register determines the field polarity of the video signal when the ENABLE pin is active.

AUTOSYNC:

0 = Auto Sync detection mode OFF
1 = Auto Sync detection mode ON (default)

VSYNCPOL and HSYNCPOL are overridden by detected sync polarity when AUTOSUNC = 1.

VSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

HSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

12.3 DISPMODE (02h)

Name	DISPMODE

Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPOFF	7	1	Display On/Off control
MONO	6	0	Mono display mode selection
GAMMA_EN	5	1	Internal Gama LUT enable
3D-MODE	4	0	3D Mode control
SCMODE	3-2	0	Progressive or Interlaced scan mode selection
VSCAN	1	0	Vertical Scan direction
HSCAN	0	0	Horizontal Scan direction

DISPOFF:

0 = Display is turned ON
1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

MONO:

0 = WHITE display mode (default)
1 = Mono display mode

The MONO is used to set monochrome display mode. When MONO = 1, the SXGA-096 only accept the input data from LVDS channel 1 and 2. Other channels (channel 0, 3) are goes to power down mode.

GAMMA_EN:

0 = Bypass Internal Gamma LUT
1 = Use internal Gamma LUT (default)

3D-MODE:

0 = Normal display mode (default)
1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE=”1” the SCMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h). The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0", bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE="1", bit #3 of the VINMODE register). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

SCMODE:

00 = Progressive scan mode (default)
01 = Interlaced scan mode
1X = Pseudo-interlaced mode

Interlaced modes are limited to a maximum of 518 and a minimum of 263 active rows per field.

VSCAN:

0 = Top to Bottom vertical scan direction (default)
1 = Bottom to Top vertical scan direction

HSCAN:

0 = Left to Right horizontal scan direction (default)
1 = Right to Left horizontal scan direction

12.4 LFTPOS (03h)

Name	LFTPOS
Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Left position of first active column

This register, along with register RGTPOS, is used to set the horizontal position of the active display window within the 1292 available columns of pixels. In SXGA mode the active window can be moved by +/-6 pixels from the center (default) position. When LFTPOS is increased, register RGTPOS must be decreased by the same value so that the sum of the two remains equal.

12.5 RGTPOS (04h)

Name	RGTPOS
Address	04h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Right position of last active column

This register, along with register LFTPOS, is used to set the horizontal position of the active display window within the 1292 available columns of pixels. In SXGA mode the active window can be moved by +/-6 pixels from the center (default) position. When RGTPOS is increased, register LFTPOS must be decreased by the same value so that the sum of the two remains equal.

12.6 TOPPOS (05h)

Name	TOPPOS
Address	05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Top position of first active row

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can be moved by +/-6 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

12.7 BOTPOS (06h)

Name	BOTPOS
Address	06h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Bottom position of last active row

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can be moved by +/-6 pixels from the center (default) position. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal.

12.8 ROWRESET (07h, 08h)

Name	ROWRESET
Address	07h, 08h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ROWRESETL (07h)	7-0	0	Row duty rate control (LSB)
ROWRESETH (08h)	1-0	0	Row duty rate control (MSB)
	4	0	ROWRESET work on UNENABLED frame in 3D mode

ROWRESETH:BIT4

0 = Active duty rate can be set 0 ~ 50%, 100% when 3D mode
1 = Active duty rate can be set 50 ~ 100% when 3D mode

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

ROWRESET (dec)	Active Line Cycles	Active Duty Rate (%)	Note
0	all	100	Pixels active for entire frame period
1	2	$2*T_{HSYNC}/T_{FRAME}$	1054 total HS cycles / frame (SXGA/60Hz)
n	2*n	$2*n*T_{HSYNC}/T_{FRAME}$	
>527	all	100	Pixels active for entire frame period

12.9 RAMPCTL (09h)

Name	RAMPCTL
Address	09h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RAMPMON	5	0	Internal RAMP Amp monitor enable
	4	0	Reserved (Do Not Change)
RAMPHIGH	3	0	Set internal RAMP DAC high
FLYBTIME	2	0	RAMP Flyback time
RAMPDLY	1-0	1	RAMP delay in DCLK cycles

RAMPMON:

0 = Disable internal RAMP Buffer monitoring (default)
1 = Enable internal RAMP Buffer monitoring

The RAMPMON register is used to enable monitoring of the internal RAMP buffer output signal.

RAMPHIGH:

0 = Normal operation (default)
1 = DAC set to all high output

The RAMPHIGH register is used to set internal RAMPDAC to all high output mode for test purposes.

FLYBTIME:

0 = 500 ns (default)
1 = 800 ns

The FLYBTIME register is used to set the fly-back (return to 0) time for the internal RAMP.

RAMPDLY:

00 = - ½ DLCK
01 = no delay (default)
10 = + ½ DCLK

The RAMPDLY2 register is used to adjust the starting position of the internal RAMP.

12.10 RAMPCM (0Ah)

Name	RAMPCM
Address	0Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RAMPBCM	7-4	4	RAMP Buffer current control
RAMPACM	3-0	4	RAMP Amp current control

RAMPBCM:

0000 = -100% (power down)
0001 = -75%
0010 = -50%
0011 = -25%
0100 = nominal (default)
0101 = +25%
0110 = +50%
0111 = +75%
…

The RAMPBCM register is used to set the operating bias current for the internal RAMP buffer. The settings reduce or increase the current by 25 % of the nominal (default) value.

RAMPACM:

0000 = -100% (power down)

0001 = -75%
0010 = -50%
0011 = -25%
0100 = nominal (default)
0101 = +25%
0110 = +50%
0111 = +75%
….

The RAMPACM register is used to set the operating bias current for the internal RAMP amplifier. The settings reduce or increase the current by 25% percentage of the nominal (default) value.

12.11 VDACMX (0Bh)

Name	VDACMX
Address	0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	80	RAMP DAC maximum value control

Register VDACMX is used to adjust the maximum value of the internal RAMP DAC signal by -40% to +40% of the nominal value.

NOTE: The normal operating value for VDACMX for the SXGA096 CF XLS should be set to 7Ah.

12.12 BIASN (0Ch)

Name	BIASN
Address	0Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
EXT_VREF	3	0	Enable external VREF
BIASN	2-0	1	Set pixel bias current

Register BIASN[2,0] sets a bias current for the OLED array in order to achieve improved control of black level and WHITE saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to a 10mW increase of power consumption for the array. It is recommended to use the BIASN=3 setting for optimal performance.

EXT_VREF:

1 = enable the external VREF source
0 = use the internal VREF source (default)

Note: This option not available on the current package – use the default setting only.

BIASN:

000 = pixel bias current is turned off
111 = pixel bias current set to maximum

12.13 GAMMASET (0Dh)

Name	GAMMASET
Address	0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PMPHOLD_EN	4	0	VCOM pump hold enable
VGNSH_EN	3	0	VGN sample & hold enable
IDSTEP	2-0	0	Current level for gamma sensor

PMPHOLD_EN:

0 = Normal operation, pump hold disabled (default)
1 = Enable pump hold during VGN sampling time

The PMPHOLD_EN register is used to disable the VCOM converter switch during the VGN sampling time to reduce noise pickup.

VGNSH_EN:

0 = Bypass the VGN sample & hold function (default)
1 = Enable the VGN sample & hold function

The VGNSH_EN register is used to activate the internal sample & hold function provided at the VGN output pin.

IDSTEP:

0h ≈ IDRF/128
1h ≈ IDRF/64
2h ≈ IDRF/32
3h ≈ IDRF/16
4h ≈ IDRF/8
5h ≈ IDRF/4
6h ≈ IDRF/2
7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

12.14 VCOMMODE (0Eh)

Name	VCOMMODE
Address	0Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISEN_EN	3-2	1	Enable the VCOM current sensor
VCOMAUTO	1-0	0	Set internal VCOM supply mode

ISEN_EN:

00 = Turn off VCOM current sensor
01/11 = Turn on VCOM current sense function

When the ISEN_EN is turned on, the internal VCOM current sense function is enabled.
If it detects overcurrent in VCOM, the internal VCOM dc-dc converter stops the pumping signal(DRV) to protect external components.

VCOMAUTO:

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
01 = AUTO2 mode (not recommended for normal operation)
10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.
In the Manual mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

12.15 VCOMCTL (0Fh)

Name	VCOMCTL
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SS_BYPASS	7	0	Bypass the VCOM soft start mode
VCKDUTY	6-4	3	VCOM clock duty control
VCKSEL	3-2	3	VCOM clock select
VCOMSS	1-0	1	VCOM soft start delay time

SS_BYPASS:

0 = Normal operation, soft-start function enabled (default)
1 = Disable the VCOM soft-start function

VCKDUTY:

0h = 1:7
1h = 1:3
2h = 3:5
3h = 1:1 (default)
4h = 5:3
5h = 3:1
6h = 7:1
7h = don’t use

Register VCKDUTY sets the VCOM clock duty ratio (high-low).

VCKSEL:

0h = 125 kHz
1h = 250 kHz

2h = 500 kHz
3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.

VCOMSS:

0h = 2 ms
1h = 4 ms (default)
2h = 8 ms
3h = 16 ms

Register VCOMSS sets the soft-start duration during startup of the VCOM converter.

12.16 VGMAX (10h)

Name	VGMAX
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VDD5 supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V. The recommended value for the SXGA096 XLS microdisplays is 0x4D.

00h = 5 (VDD5 = 5V)
0Dh = 4.95 (default)
FFh = 4

VGMAX level = VDD5*(1 - 0.2*VGMAX(dec) / 255)

12.17 VCOM (11h)

Name	VCOM
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	**51***	40	30
Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	**-2.4**	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE =01. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply ≈ -2.3V.

12.18 IDRF (12h)

Name	IDRF
Address	12h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
IDRF_FINE	4-0	0	Fine adjustment for array reference current

IDRF_COARSE:

IC#
0h = 0 (default)
1h = 0.5
2h = 1.5
3h = 2.5
4h = 3.5

IDRF_FINE:

IF#
00h = 0 (default)
01h = 1/32

…
10h = 16/32
…
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF given by the following expression:

LMAX = LDEF*(IC# + IF#) in cd/m^2

where the luminance for a WHITE display is LDEF ≈ $600cd/m^2$ at the recommended settings (see table below).

IDRF (hex)	LMAX / LDEF
0	0
10	0.5
20	0.5
30	1 (recommended)
40	1.5
50	2
60	2.5
70	3
80	3.5

This register is only operational in Auto VCOM mode (VCOMMODE=00).

12.19 DIMCTL (13h)

Name	DIMCTL
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	1	Dimming level control

00h = 0
01h = 1% of LMAX
…
64h = 100% of LMAX
…
7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The recommended value of 64h is equal to 100% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

12.20 TREFDIV (14h)

Name	TREFDIV
Address	14h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	17	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

12.21 TEMPOFF (15h)

Name	TEMPOFF
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	3A	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

12.22 TUPDATE (16h)

Name	TUPDATE
Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description

	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

Update Time = (TUPDATE(decimal) + 1)*T_{FRAME}

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

12.23 TEMPOUT (17h)

Name	TEMPOUT
Address	17h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature.

$$T(°C) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60ºC will return a TEMPOUT reading of 0 and temperatures above +80ºC will return a hexadecimal value of FF.

12.24 ANGPWRDN (18h)

Name	ANGPWRDN
Address	18h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISENPD	7	0	ISEN power down
IDMAXPD	6	0	IDMAX power down
VCOMPD	5	0	VCOM power down
VREFPD	4	0	VREF power down
GMSENPD	3	0	Gamma sensor power down
VCSENPD	2	0	VCOM sensor power down
TSENPD	1	0	Temperature sensor power down
TREFPD	0	0	Temperature reference power down

ISENPD:

1 = VCOM current limit sensor is powered down
0 = normal operation (default)

IDMAXPD:

1 = IDMAX function is powered down
0 = normal operation (default)

VCOMPD:

1 = VCOM generator is powered down
0 = normal operation (default)

VREFPD:

1 = the VREF reference source is powered down
0 = normal operation (default)

GMSENPD:

1 = the Gamma sensor is powered down
0 = normal operation (default)

VCSNEPD:

1 = the VCOM sensor is powered down
0 = normal operation (default)

TSENPD:

1 = the Temperature Sensor is powered down
0 = the Temperature Sensor is operating normally (default)

TREFPD:

1 = the Temperature reference is powered down
0 = normal operation (default)

12.25 SYSPWRDN (19h)

Name	SYSPWRDN
Address	19h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PDWN	7	0	All systems power down
LVDSPD	6	0	LVDS receiver power down
LDOPD	5	0	1.8V LDO power down
RBUFPD	4	0	RAMP Buffer Power Down
RAMPPD	3	0	RAMP DAC amp and buffer power down
DACPD	2	0	RAMP DAC power down
POR50VPD	1	0	5V power-on-reset power down
POR18VPD	0	0	2.5V power-on-reset power down

PDWN:

1 = all systems are powered down
0 = normal operation (default)

By setting the PDWN bit with LDOPD bit to a "1" the chip enters a deep sleep mode in which all functions including the I^2C interface are powered down in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I^2C input lines and resets the PDWN bit when it detects the correct I^2C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

LVDSPD:
1 = LVDS receiver is powered down
0 = normal operation (default)

LDOPD:
1 = 1.8V LDO is powered down
0 = 1.8V LDO is enabled (default)

It is recommended not to use the internal 1.8V LDO, so the LDOPD bit should be set to "1" when powering up the display.

RBUFPD:

1 = internal RAMP buffer is powered down
0 = normal operation (default)

RAMPPD:

1 = internal RAMP DAC amplifier is powered down
0 = normal operation (default)

DACPD:

1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

POR50VPD:

1 = the 5V power-on-reset circuit is powered down
0 = normal operation (default)

POR18VPD:

1 = the 1.8V power-on-reset circuit is powered down
0 = normal operation (default)

12.26 TPMODE (1Ah)

Name	TPMODE
Address	1Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TPVCLK	4	0	Enable external clock in Burn-in mode
PATTEN	3	0	Enable test pattern display
PATTSEL	2-0	0	Select test pattern for Burn-In mode

TPVCLK:

0 = Internal ring oscillator is used for test pattern generation (default)
1 = Test pattern generator use the external clock which is LVDS clock

The BI pin is tied high or PATTEN register set to high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)
001 = WHITE bars
010 = gray scale (without gamma correction)
011 = checkerboard pattern
100 = alternating columns pattern
101 = alternating rows pattern
110 = grid pattern
101 = all black
111 = WHITE screen based on TPWHITE register value.

12.27 TPLINWTH (1Bh)

Name	TPLINWTH
Address	1Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern line width

This register is used to set the line width for the line-type test patterns.

0 = 1 pixel wide (default)
1 = 2 pixel wide
…
255 = 256 pixel wide

12.28 TPCOLSP (1Ch)

Name	TPCOLSP
Address	1Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern column spacing

This register is used to set the column spacing for the column-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

12.29 TPROWSP (1Dh)

Name	TPROWSP
Address	1Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern row spacing

This register is used to set the row spacing for the row-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

12.30 TPWHITE (1Eh)

Name	TPWHITE
Address	1Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7:0	0	Test pattern WHITE or 256 gray level

This register is used to set the background and foreground WHITEs (RGB) for certain test patterns. When PATTSEL is selected to 4,5,or 6, bit2:0 is used as foreground WHITE and bit 6:4 as background WHITE.
All 8 bits data is applied to RGB data for one of 256 grey level when PATTSEL is selected to 7.

12.31 DLYSEL (1Fh)

Name	DLYSEL
Address	1Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKWDLY	7-4	0	LVDS skew align reference clock delay
CLKDLY	3-0	1	LVDS clock delay for serial data latch

SKWDLY :

0 = Base delay
1 = Base delay + 1 unit delay
…
15 = Base delay + 15 unit delay

CLKDLY :
0 = Base delay
1 = Base delay + 1 unit delay
…
15 = Base delay + 15 unit delay

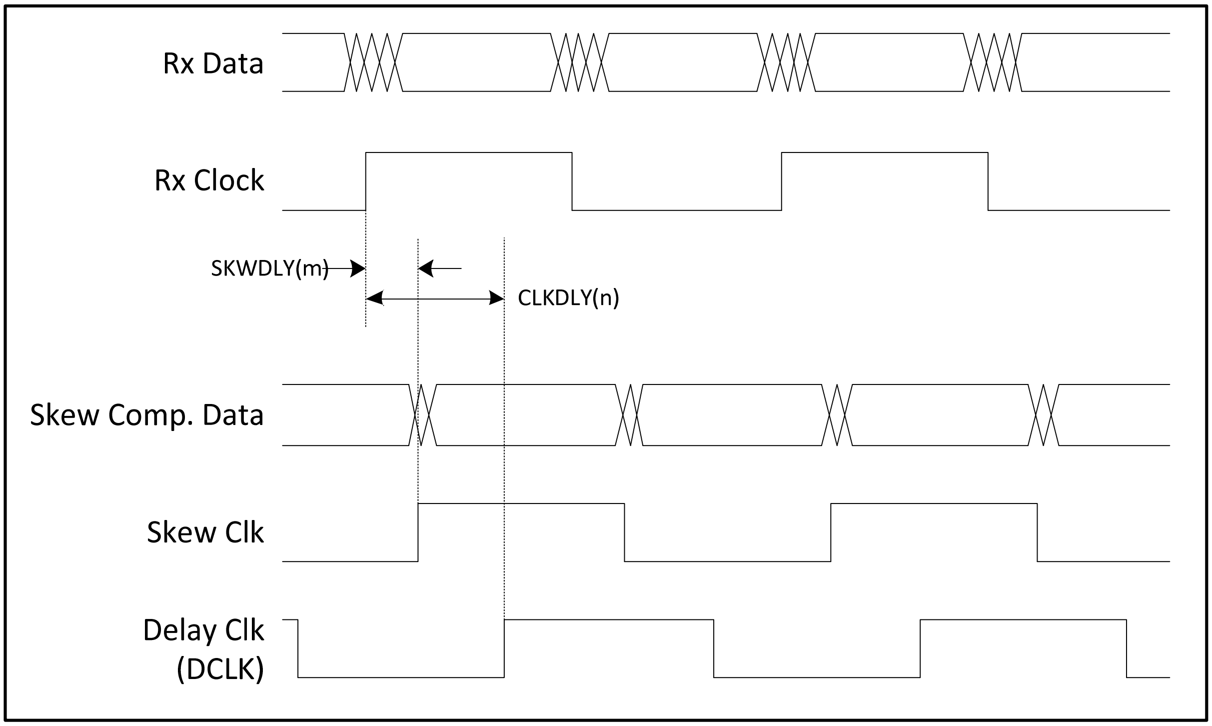


Figure 36 : LVDS Skew compensation timing diagram

12.32 LVDSCTL (20h)

Name	LVDSCTL
Address	20h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ALNMOD	2	0	Enable LVDS align mode
SKEWMOD	1-0	0	Select skew compensation mode

ALNMOD :
1 = Enable LVDS align mode

- LVDS Tx should send proper align pattern (10000000) on LVDS_DAT1 with ALIGN signal
- Don't set with SKEWMOD = 1 (auto skew compensation mode)

0 = Disable LVDS align mode (stay current align setting and any ALIGN and align pattern input are ignored)

ALNMOD should set after activate ALIGN signal and reset before deactivate ALIGN signal. It is recommended to use free running HSYNC as ALIGN signal.

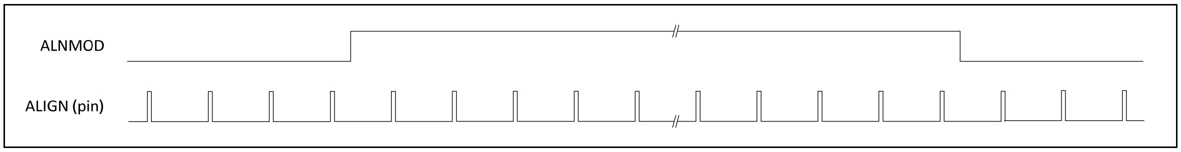


Figure 37 : ALIGN signal example

SKEWMOD:

0 = Normal operation mode (stays current skew delay setting and no change)
1 = Automatic skew delay setting mode

- LVDS Tx should send proper Skew compensation pattern (00001111) on all data and clock

2 = Manual common skew delay setting mode (SKEW1 delay setting is used on all data line delay)
3 = Manual separate skew delay setting mode

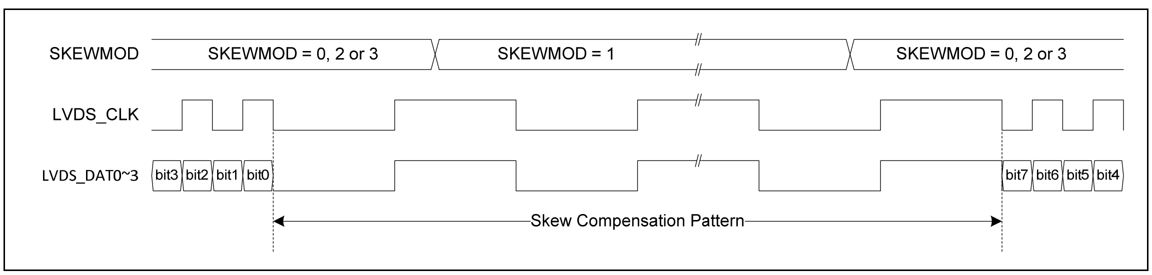


Figure 38 : Skew compensation pattern

The SKEWMOD register operation is only valid while LVDS TX is sending the skew compensation pattern.

12.33 SKEW0 (21h, 22h)

Name	SKEW0
Address	21h, 22h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW0(21h)	7-0	0	data line #0 delay setting lower byte

SKEW0 (22h)	15-8	0	data line #0 delay setting upper byte

00000000 00000000 = Base delay setting
00000000 00000001 = Base + 1 unit delay setting
00000000 00000011 = Base + 2 unit delay setting
00000000 00000111 = Base + 3 unit delay setting
00000000 00001111 = Base + 4 unit delay setting
:
01111111 11111111 = Base + 14 unit delay setting
11111111 11111111 = Base + 15 unit delay setting

I^{2}C register SKEW0~SKEW3 read out are always current working delay value

- SKEWMOD = 0 or 1 : current auto skew compensated values are read
- SKEWMOD = 2 : SKEW0 register value is applied to all other skew resister and read on all SKEW0~SKEW3
- SKEWMOD = 3 : each SKEWi register values are applied and read

12.34 SKEW1 (23h, 24h)

Name	SKEW1
Address	23h, 24h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW1 (24h)	7-0	0	data line #1delay setting lower byte
SKEW1 (25h)	15-8	0	data line #1 delay setting upper byte

12.35 SKEW2 (25h, 26h)

Name	SKEW2
Address	25h, 26h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW2 (25h)	7-0	0	data line #2 delay setting lower byte
SKEW2 (25h)	15-8	0	data line #2 delay setting upper byte

12.36 SKEW3 (27h, 28h)

Name	SKEW3
Address	27h, 28h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SKEW3 (27h)	7-0	0	data line #3 delay setting lower byte

SKEW3 (28h)	15-8	0	data line #3 delay setting upper byte

12.37 SKFAST (29h)

Name	SKFAST
Address	29h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
SKFAST	3-0	-	All "0' after skew compensation => OK

Bit 15 of SKEW0 ~ SKEW3. If any of SKFAST bit is read as "1" after skew compensation then that line comes much faster than selected skew clock. Decrease SKWDLY setting if possible.

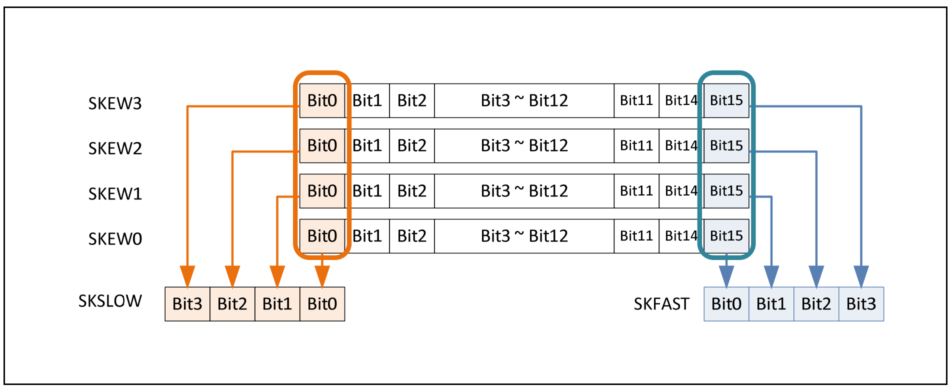


Figure 39 : SKFAST and SKSLOW register mapping

12.38 SKSLOW (2Ah)

Name	SKSLOW
Address	2Ah
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
SKSLOW	3-0	0	All "1" after skew compensation => OK

Bit 0 of SKEW0 ~ SKEW3. If any of SKSLOW bit is read as "0" after skew compensation then that line comes to much slower than selected skew clock. Increase SKWDLY setting if possible.

12.39 SYNCMOD (2Bh)

Name	SYNCMOD
Address	2Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DEFEN	2-1	1	Define ENABLE pin function
DEFHS	0	0	Define LVDS_ALGN pin function

DEFEN:
- 0 = Do not use ENABLE pin (ENABLE & VSYNC signal uses thru LVDS data lines)
- 1 = ENABLE pin used as ENABLE (Default)
- 2 = ENABLE pin used as VSYNC
- 3 = Do not use

DEFHS:
- 0 = LVDS_ALGN pin used as ALIGN function
- 1 = LVDS_ALGN pin used as ALIGN & HSYNC function

12.40 LUT_ADDR (2Ch)

Name	LUT_ADDR
Address	2Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_ADDR	7-0	0	Gamma look-up table template access address

12.41 LUT_DATA (2Dh, 2Eh)

Name	LUT_DATA
Address	2Dh, 2Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_DATAL (2Dh)	7-0	0	Gamma look-up table template R/W data LSB
LUT_DATAH (2Eh)	9-8	0	Gamma look-up table template R/W data MSB

When LUT_DATAL(2Dh) register is written following operations are happen
- Write Gamma look-up table template memory to LUT_DAT (10bit) data at current LUT_ADDR address
- Increase LUT_ADDR register by 1 after write operation

When LUT_DATA register are read following data are read

- Current LUT_ADDR address data of Gamma look-up table memory are read

12.42 LUT_UPDATE (2Fh)

Name	LUT_UPDATE
Address	2Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
UDGAMMA	3	0	Update LUT template to R,G,B LUT memory
UDRGB	2-0	7	Select R,G,B Gamma LUT for Update

UDGAMMA:
  0 = No operations happen
  1 = Enable copy LUT template memory data to selected R,G,B Gamma LUT memory
UDGAMMA register operation

- R,G,B LUT memory update is started at first VSYNC rising edge meet after UDGAMMA register set to 1
- UDGAMMA register cleared to 0 after update operation end automatically

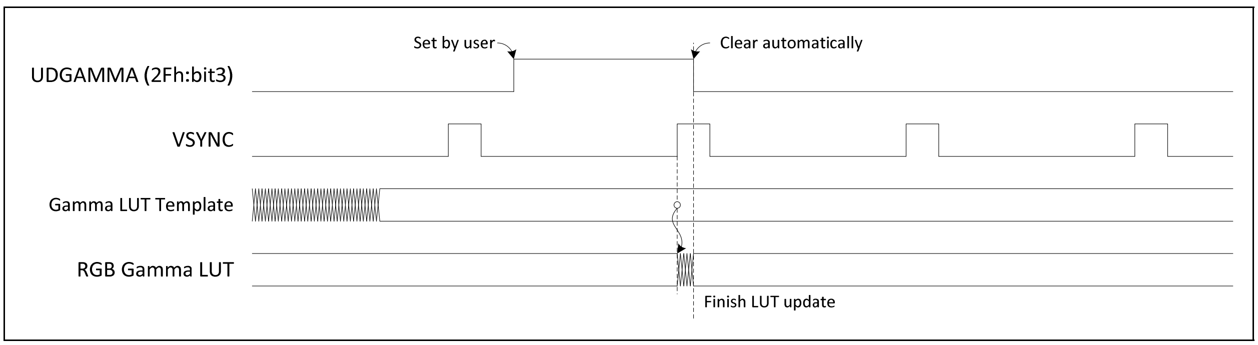


Figure 40 : Gamma LUT Update timing

UDRGB:
  001 = Select B Gamma LUT memory updated
  010 = Select G Gamma LUT memory updated
  011 = Select G, B Gamma LUT memory updated
  100 = Select R Gamma LUT memory updated
  101 = Select R, B Gamma LUT memory updated
  110 = Select R, G Gamma LUT memory updated
  111 = Select R, G, B Gamma LUT memory updated

12.43 Reserved (30h,31h,32h,33h)

Name	Reserved
Address	30h,31h,32h,33h
Mode	Read

Bit Name	Bit#	Reset Value	Description
	7-0	-	Reserved

12.44 Reserved (34h,35h)

Name	Reserved
Address	34h,35h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	99	Reserved (Do Not Change)

12.45 Reserved (36h)

Name	Reserved
Address	36h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	3-0	0	Reserved (Do Not Change)

12.46 Reserved (37h)

Name	Reserved
Address	37h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	0	Reserved (Do Not Change)

12.47 Reserved (38h,39h)

Name	Reserved

Address	38h,39h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved (Do Not Change)

12.48 Reserved (3Ah)

Name	Reserved
Address	3Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Reserved (Do Not Change)

12.49 Reserved (3Bh)

Name	Reserved
Address	3Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Reserved (Do Not Change)

12.50 Reserved (3Ch)

Name	Reserved
Address	3Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	4-0	0	Reserved (Do Not Change)

12.51 Reserved (3Dh)

Name	Reserved
Address	3Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	2-0	3	Reserved (Do Not Change)

12.52 Reserved (40h)

Name	Reserved
Address	40h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	0	Reserved (Do Not Change)

12.53 Reserved (41h)

Name	Reserved
Address	41h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	30	Reserved (Do Not Change)

12.54 Reserved (42h)

Name	Reserved
Address	42h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	64	Reserved (Do Not Change)

13. APPENDIX A: APPLICATION SYSTEM DIAGRAM

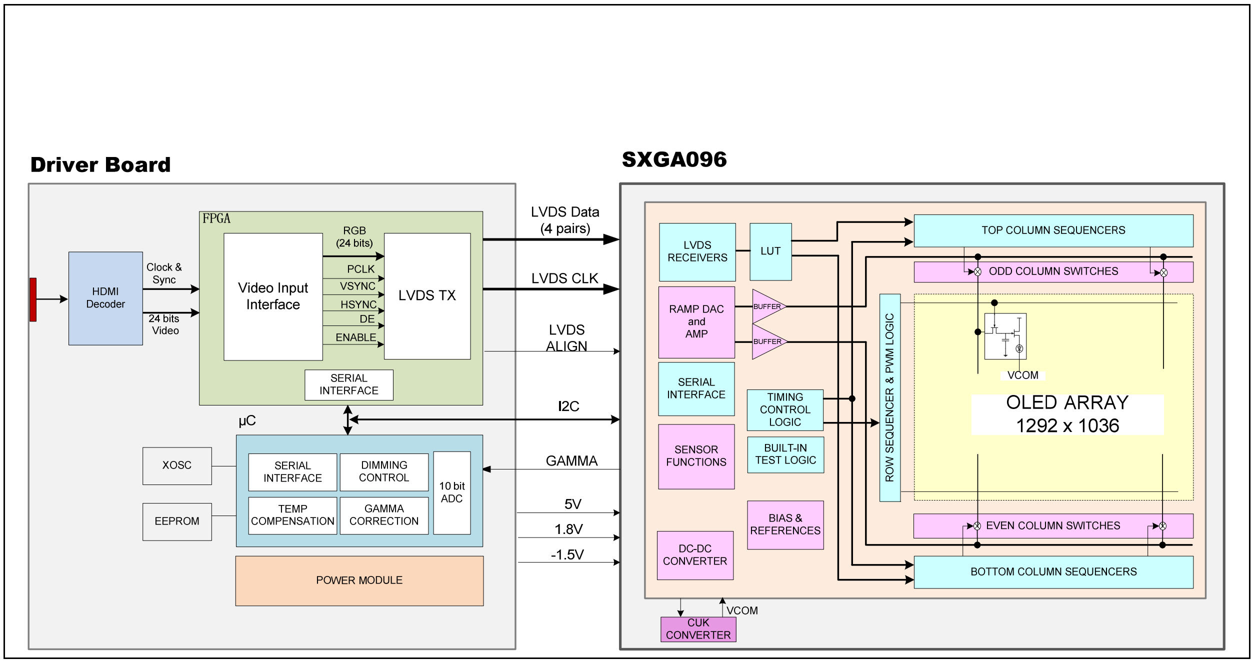


Figure 41 : Block diagram of application reference system

14. APPENDIX B: LVDS TX DESIGN EXAMPLE

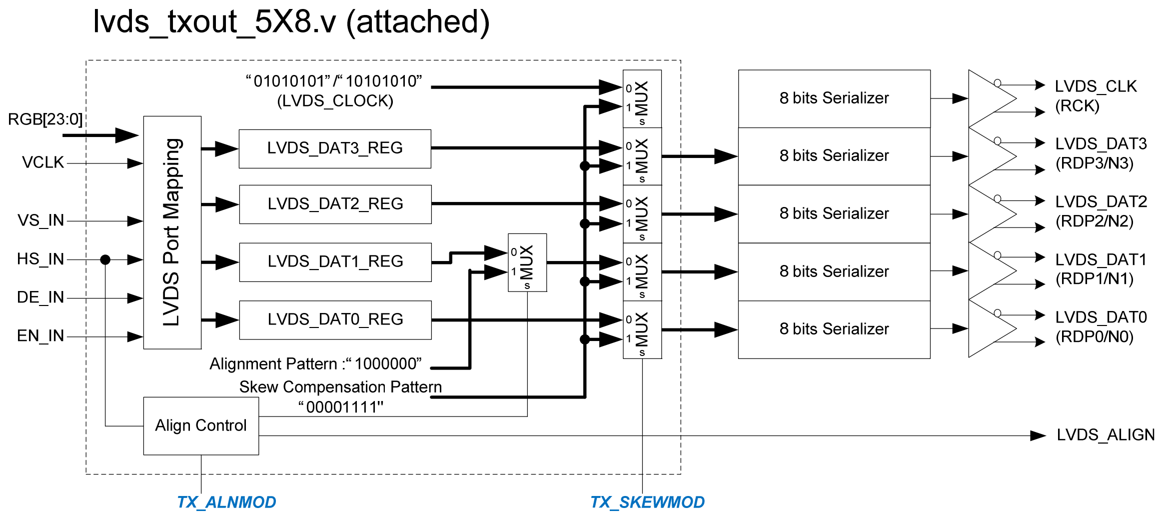


Figure 42 : LVDS TX Reference Design

The LVDS TX module should have two I2C registers, which are TX_ALNMOD and TX_SKEWMOD since LVDS RX requires special alignment and skew compensation patterns. ALNMOD Register : When it is set, the TX should send the alignment pattern via 2nd LVDS data channel (LVDS_DAT1) and LVDS_ALIGN signal which is a CMOS output. The alignment pattern is: "10000000".

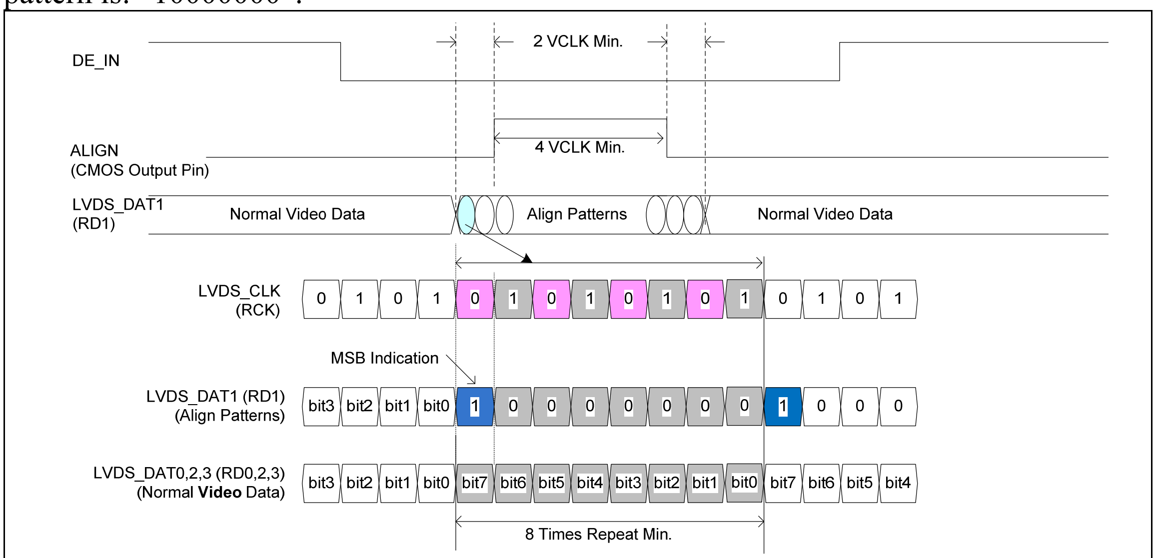


Figure 43 : LVDS Alignment Pattern and Timing

SKEWMOD Register : When it is set, the TX should send the skew compensation patterns through all of the LVDS channel including the clock channel. The skew compensation pattern is "0001111".

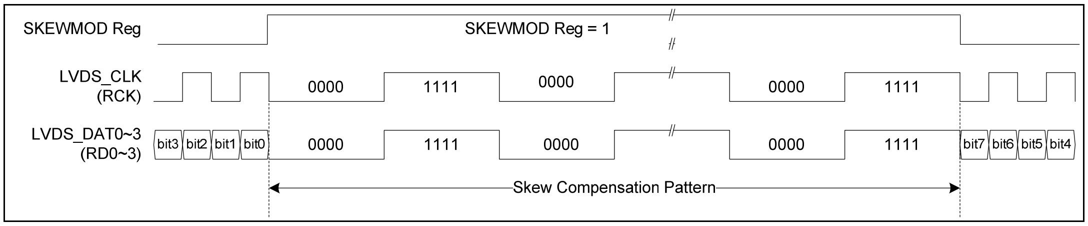


Figure 44 : LVDS Skew Compensation Pattern and Timing

Example RTL Code for LVDS_TXOUT_5X8.v

```
// Created Tue Nov 26 11:31:11 2013
//-----------------------------------------------------------------------------------------------
//
// Title       : LVDS_TXOUT_5X8
// Design      : SXGA096_FPGA
// Author      : Jae Koh
// Company     : eMagin
//
//-----------------------------------------------------------------------------------------------
`timescale 1ns / 10ps

module LVDS_TXOUT_5X8 ( HS_IN ,HS_OUT ,rstn ,DIN ,EN_IN ,EN_OUT ,clk ,DOUT
          ,DE_IN ,VS_IN ,LVDSCTL ,LVDS_HS ,VS_OUT ,DE_OUT );

          input EN_IN ;
          wire EN_IN ;
          input HS_IN ;
          wire HS_IN ;
          input [23:0] DIN ;
          wire [23:0] DIN ;
          input clk ;
          wire clk ;
          input VS_IN ;
          wire VS_IN ;
          input DE_IN ;
          wire DE_IN ;
          input rstn ;
          wire rstn ;
          input [1:0] LVDSCTL ;         // {ALNMOD, SKWMOD}
          wire [1:0] LVDSCTL ;

          output EN_OUT ;
          wire EN_OUT ;
          output HS_OUT ;
          wire HS_OUT ;
          output VS_OUT ;
          wire VS_OUT ;
          output DE_OUT ;
          wire DE_OUT ;
          output [39:0] DOUT ;
          reg [39:0] DOUT ;
          output LVDS_HS ;
          reg LVDS_HS ;

          reg [87:0] DOUT0 ;
          reg [4:0] VSO, DEO, ENO;
          reg [7:0] HSO;
          wire ALGN;
          wire ALNMOD = LVDSCTL[1];
          wire SKWMOD = LVDSCTL[0];

          assign EN_OUT = ENO[4];
          assign VS_OUT = VSO[4];
          assign HS_OUT = HSO[4];
          assign DE_OUT = DEO[4];

          assign ALGN = ~DE_IN & (HS_IN | HSO[3] | HSO[7]) & ALNMOD;

          wire [7:0] RIN, GIN, BIN;

          assign RIN = DIN[23:16];
          assign GIN = DIN[15:8];
          assign BIN = DIN[7:0];

          always @(DOUT0)
                    begin
                              // LVDS_CLK
                              DOUT[39] <= DOUT0[39];
                              DOUT[38] <= DOUT0[38];
                              DOUT[37] <= DOUT0[37];
                              DOUT[36] <= DOUT0[36];
                              DOUT[35] <= DOUT0[35];
                              DOUT[34] <= DOUT0[34];
                              DOUT[33] <= DOUT0[33];
                              DOUT[32] <= DOUT0[32];
                              // LVDS_D[3]
                              DOUT[31] <= DOUT0[31];
                              DOUT[30] <= DOUT0[30];
                              DOUT[29] <= DOUT0[29];
                              DOUT[28] <= DOUT0[28];
                              DOUT[27] <= DOUT0[27];
                              DOUT[26] <= DOUT0[26];
                              DOUT[25] <= DOUT0[25];
                              DOUT[24] <= DOUT0[24];
                              // LVDS_D[2]
                              DOUT[23] <= DOUT0[23];
                              DOUT[22] <= DOUT0[22];
                              DOUT[21] <= DOUT0[21];
                              DOUT[20] <= DOUT0[20];
                              DOUT[19] <= DOUT0[19];
```

```
                    DOUT[18] <= DOUT0[18];
                    DOUT[17] <= DOUT0[17];
                    DOUT[16] <= DOUT0[16];
                    // LVDS_D[1]
                    DOUT[15] <= DOUT0[15];
                    DOUT[14] <= DOUT0[14];
                    DOUT[13] <= DOUT0[13];
                    DOUT[12] <= DOUT0[12];
                    DOUT[11] <= DOUT0[11];
                    DOUT[10] <= DOUT0[10];
                    DOUT[9]  <= DOUT0[9];
                    DOUT[8]  <= DOUT0[8];
                    // LVDS_D[0]
                    DOUT[7]  <= DOUT0[7];
                    DOUT[6]  <= DOUT0[6];
                    DOUT[5]  <= DOUT0[5];
                    DOUT[4]  <= DOUT0[4];
                    DOUT[3]  <= DOUT0[3];
                    DOUT[2]  <= DOUT0[2];
                    DOUT[1]  <= DOUT0[1];
                    DOUT[0]  <= DOUT0[0];
          end

always @(negedge rstn or negedge clk)
          if (!rstn)
                    LVDS_HS <= 0;
          else
                    LVDS_HS <= HSO[2];

always @(negedge rstn or posedge clk)
          if (!rstn)
                    begin
                              VSO <= 0;
                              HSO <= 0;
                              DEO <= 0;
                              ENO <= 0;
                              DOUT0 <= 0;
                    end
          else
                    begin
                              VSO <= {VSO[3:0], VS_IN};
                              HSO <= {HSO[6:0], HS_IN};
                              DEO <= {DEO[3:0], DE_IN};
                              ENO <= {ENO[3:0], EN_IN};

                              if (SKWMOD)
                                        begin
                                                  DOUT0 <= 40'h0F0F0F0F0F;
                                        end
                              else
                                        begin
                                                  DOUT0[39:32] <= 8'b01010101;
                                                  // RD3P/RD3N
                                                  DOUT0[31] <= BIN[5];
                                                  DOUT0[30] <= BIN[4];
                                                  DOUT0[29] <= BIN[3];
                                                  DOUT0[28] <= BIN[1];
                                                  DOUT0[27] <= BIN[0];
                                                  DOUT0[26] <= BIN[2];
                                                  DOUT0[25] <= BIN[6];
                                                  DOUT0[24] <= ~BIN[6];
                                                  // RD2P/RD2N
                                                  DOUT0[23] <= RIN[0];
                                                  DOUT0[22] <= DE_IN;
                                                  DOUT0[21] <= HS_IN;
                                                  DOUT0[20] <= EN_IN;
                                                  DOUT0[19] <= VS_IN;
                                                  DOUT0[18] <= BIN[7];
                                                  DOUT0[17] <= GIN[7];
                                                  DOUT0[16] <= ~GIN[7];
                                                  // RD1P/RD1N
                                                  if (ALGN)
                                                            begin
                                                                      DOUT0[15] <= 1;
                                                                      DOUT0[14] <= 0;
                                                                      DOUT0[13] <= 0;
                                                                      DOUT0[12] <= 0;
                                                                      DOUT0[11] <= 0;
                                                                      DOUT0[10] <= 0;
                                                                      DOUT0[9] <= 0;
                                                                      DOUT0[8] <= 0;
                                                            end
                                                  else
                                                            begin
                                                                      DOUT0[15] <= GIN[6];
                                                                      DOUT0[14] <= GIN[5];
                                                                      DOUT0[13] <= GIN[1];
                                                                      DOUT0[12] <= GIN[0];
                                                                      DOUT0[11] <= GIN[4];
                                                                      DOUT0[10] <= GIN[3];
                                                                      DOUT0[9] <= GIN[2];
                                                                      DOUT0[8] <= ~GIN[2];
                                                            end
                                                  // RD0P/RD0N
```

```
                                                DOUT0[7] <= RIN[7];
                                                DOUT0[6] <= RIN[1];
                                                DOUT0[5] <= RIN[6];
                                                DOUT0[4] <= RIN[5];
                                                DOUT0[3] <= RIN[4];
                                                DOUT0[2] <= RIN[3];
                                                DOUT0[1] <= RIN[2];
                                                DOUT0[0] <= ~RIN[2];
                                        end
                        end

endmodule
```

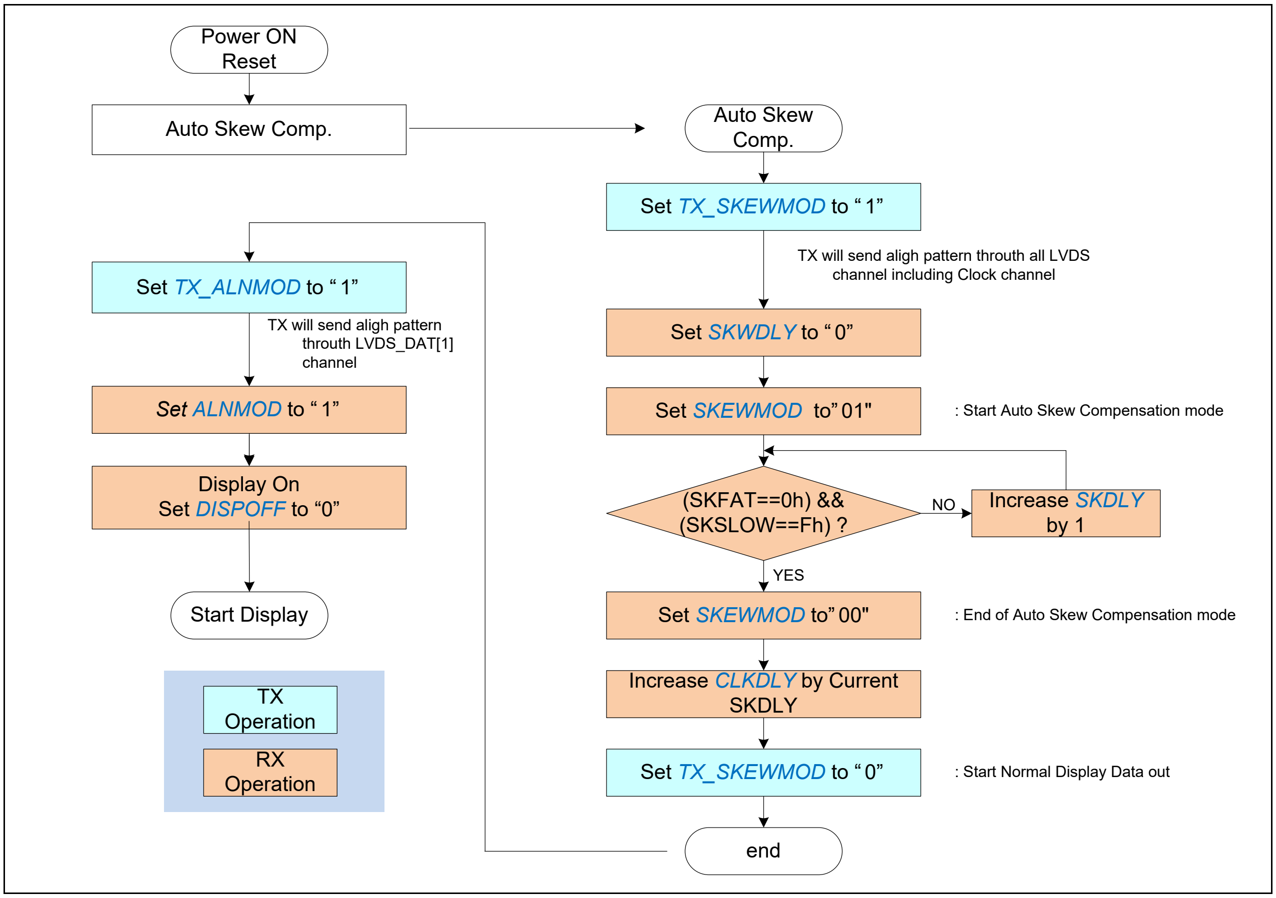


Figure 45 : LVDS Link Setup Flow Chart for Firmware

15. APPENDIX C: EEPROM MEMORY MAP

Each SXGA096 micro display contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I^{2}C serial interface that is used to communicate with the micro display. The EEPROM'S serial address is as follows:

SERADD = 0
Write Mode: Address is A6h
Read Mode: Address is A7h

SERADD = 1
Write Mode: Address is AEh
Read Mode: Address is AFh

The first 15 bytes represent the serial number of the SXGA096 micro display. The following 68 bytes contain sequential data values that can be used to write to the micro display's internal registers starting with eeprom address 16 to 84.

Addresses 00 to 15 (decimal) should not be changed as they contain serial number and traceability information

Addresses 34, 36, 37,141, 142 to145 contain calibrated values specific to each display and should not be changed

Address 34 contains the IDRF value needed to reach 150 cd/m^2 at room ambient
Addresses 36 and 37 contain the on-chip temperature sensor calibration values, needed to correctly measure the display temperature
Addresses 142-145 contain the information needed to calculate the IDRF needed set an absolute luminance (in cd/m^2) .

Registers defined as RESERVED should not be changed.

Addresses beyond 91h are blank and may be used.

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

Memory Addr (Dec)	Memory Addr (hex)	EEPROM Data	Memory Addr (Dec)	Memory Addr (hex)	EEPROM Data
0	0	Serial Char #0	43	2B	TPLINWTH
1	1	Serial Char #1	44	2C	TPCOLSP
2	2	Serial Char #2	45	2D	TPROWSP
3	3	Serial Char #3	46	2E	TPCOLOR
4	4	Serial Char #4	47	2F	DLYSEL
5	5	Lot Char#0	48	30	LVDSCTL
6	6	Lot Char#1	49	31	SKEW0L
7	7	Lot Char#2	50	32	SKEW0H
8	8	Lot Char#3	51	33	SKEW1L
9	9	Lot Char#4	52	34	SKEW1H
10	A	Lot Char#5	53	35	SKEW2L
11	B	Wafer Char#0	54	36	SKEW2H
12	C	Wafer Char#1	55	37	SKEW3L
13	D	Wafer Char#2	56	38	SKEW3H
14	E	Wafer Char#3	57	39	SKFAST
15	F	Data Format Version# (00h)	58	3A	SKSLOW
16	10	STAT	59	3B	SYNCMOD
17	11	VINMODE	60	3C	LUT_ADDR
18	12	DISPMODE	61	3D	LUT_DATA_L
19	13	LFTPOS	62	3E	LUT_DATA_H
20	14	RGTPOS	63	3F	LUT_UPDATE
21	15	TOPPOS	64	40	NOFPIXELL
22	16	BOTPOS	65	41	NOFPIXELH
23	17	ROWRESETL	66	42	NOFLINEL
24	18	ROWRESETH	67	43	NOFLINEH
25	19	RAMPCTL	68	44	NVCK0
26	1A	RAMPCM	69	45	NVCK1
27	1B	VDACMX	70	46	PUPCTL
28	1C	BIASN	71	47	HIDNCTL
29	1D	GAMMASET	72	48	DIGTEST
30	1E	VCOMMODE	73	49	Reserved
31	1F	VCOMCTL	74	4A	Reserved
32	20	VGMAX	75	4B	Reserved
33	21	VCOM	76	4C	Reserved
34	22	IDRF	77	4D	Reserved
35	23	DIMCTL	78	4E	Reserved
36	24	TREFDIV	79	4F	DISPMOD_BN
37	25	TEMPOFF	80	50	IDRF_BN
38	26	TUPDATE	81	51	DIMCTL_BN
39	27	TEMPOUT	82	52	Reserved
40	28	ANGPWRDN	83	53	Reserved
41	29	SYSPWRDN	84	54	Reserved
42	2A	TPMODE	85	55	VGNA0_HI

Memory Addr (Dec)	Memory Addr (hex)	EEPROM Data
86	56	VGNA0_LO
87	57	VGNA1_HI
88	58	VGNA1_LO
89	59	VGNA2_HI
90	5A	VGNA2_LO
91	5B	VGNA3_HI
92	5C	VGNA3_LO
93	5D	VGNA4_HI
94	5E	VGNA4_LO
95	5F	VGNA5_HI
96	60	VGNA5_LO
97	61	VGNA6_HI
98	62	VGNA6_LO
99	63	VGNA7_HI
100	64	VGNA7_LO
101	65	VGNB0_HI
102	66	VGNB0_LO
103	67	VGNB1_HI
104	68	VGNB1_LO
105	69	VGNB2_HI
106	6A	VGNB2_LO
107	6B	VGNB3_HI
108	6C	VGNB3_LO
109	6D	VGNB4_HI
110	6E	VGNB4_LO
111	6F	VGNB5_HI
112	70	VGNB5_LO
113	71	VGNB6_HI
114	72	VGNB6_LO
115	73	VGNB7_HI
116	74	VGNB7_LO
117	75	GMMA00_HI
118	76	GMMA00_LO
119	77	GMMA01_HI
120	78	GMMA01_LO
121	79	GMMA02_HI
122	7A	GMMA02_LO
123	7B	GMMA03_HI
124	7C	GMMA03_LO
125	7D	GMMA04_HI
126	7E	GMMA04_LO
127	7F	GMMA05_HI
128	80	GMMA05_LO

Memory Addr (Dec)	Memory Addr (hex)	EEPROM Data
129	81	GMMA06_HI
130	82	GMMA06_LO
131	83	GMMA07_HI
132	84	GMMA07_LO
133	85	Blank
134	86	Blank
135	87	Blank
136	88	Blank
137	89	MM
138	8A	DD
139	8B	YY
140	8C	YY
141	8D	Blank
142	8E	High-Slope1 (int)
143	8F	High-Slope2 (frac)
144	90	High-Origin_H
145	91	High-Origin_L
146	92	Low-Slope1 (int)
147	93	Low-Slope2 (frac)
148	94	Low-Origin_H
149	95	Low-Origin_L

16. APPENDIX D: RECOMMENDED REGISTER SETTINGS

Below are the recommended settings for luminance levels greater than ~ 700-900 cd/m^2

Address	Name	Value	Address	Name	Value
00h	STATUS	00	21h	SKEW0L	00
01h	VINMODE	07	22h	SKEW0H	00
02h	DISPMODE	20	23h	SKEW1L	00
03h	LFTPOS	06	24h	SKEW1H	00
04h	RGTPOS	06	25h	SKEW2L	00
05h	TOPPOS	06	26h	SKEW2H	00
06h	BOTPOS	06	27h	SKEW3L	00
07h	ROWRSTL	00	28h	SKEW3H	00
08h	ROWRSTH	00	29h	SKFST	00
09h	RAMPCTL	01	2Ah	SKSLW	00
0Ah	RAMPCM	44	2Bh	SYNCMD	02
0Bh	VDACMX	80	Ch	LUT_ADR	00
0Ch	BIASN	3	2Dh	LUTDL	00
0Dh	GAMMST	07	2Eh	LUTDH	00
0Eh	VCOMMODE	04	2Fh	LUT_UP	07
0Fh	VCOMCTL	29	30h	RES	00
10h	VGMAX	4D	31h	RES	05
11h	VCOM	51	32h	RES	00
12h	IDRF	70	33h	RES	04
13h	DIMCTL	64	34h	NVCK0	99
14h	TREFDIV	17	35h	NVCK1	99
15h	TMPOFF	40	36h	RES	00
16h	TUPDATE	10	37h	RES	00
17h	TEMPOUT	98	38h	RES	00
18h	ANGPRDN	00	39h	RES	00
19h	SYSPRDN	01	3Ah	RES	FF
1Ah	TPMODE	02	3Bh	RES	00
1Bh	TPLNWTH	03	3Ch	RES	00
1Ch	TPCOLSP	04	3Dh	RES	03
1Dh	TPROSP	00	3Eh	RES	00
1Eh	TPCOLOR	07	3Fh	RES	00
1Fh	DLYSEL	12	40h	RES	00
20h	LVDSCTL	04	41h	IDRF-BN	30
			42h	DIMCTL-DN	64